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Generalised hybrid switching topology for a single-phase modular multilevel inverter

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Abstract: A modified single-phase hybrid cascaded H bridge multilevel inverter with a minimum number of power electronic devices and isolated DC sources is presented in this study. It consists of two inverters (upper and lower) coupled in cascade. The lower inverter is capable of developing a multilevel output and switches at low frequency and another inverter develops two-level output and switches at high frequency. In the proposed inverter, every additional power electronic switch in the lower inverter increases the level by four. This study also introduces a generalised hybrid modulation switching strategy, which gives arithmetical and logical expressions for switching the additional device for any required increase in levels. The voltage rating of the devices, conduction and switching loss of the proposed inverter are compared with the similarly setup topologies. The generalised hybrid modulation algorithm is simulated in MATLAB/Simulink and implemented in a SPATRAN 3A DSP board. Simulation and experimental results are presented for different loading conditions.

1 Introduction

During the last few decades, technological improvement in power electronic devices and increasing demand for energy have contributed to hasty development of power generation based on renewable energy sources. Photovoltaic (PV), wind and fuel cell (FC)-based renewable energy technologies are paying attention among the researchers over the globe [1–7].

One of the tribulations focused in the research is the limitation of power electronic switches. If the power electronic devices that can withstand high voltage are used in the inverter, their switching frequency is restricted. Hence, the device voltage must be decreased to use fast switching devices. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels [8].

Moreover, increase in number of isolated DC sources increases the number of output voltage levels. But this makes the system more complex, particularly in PV and FC fed inverter topologies. DC–DC converters are mandatory for each isolated DC source in PV or FC applications. These converters adjust the variable or low-quality output voltage of PV or FC stacks. In addition, power output of PV and FC stacks has to be maximised as it depends on the ecological factors. So in order to track the maximum power point of PV string or FC stacks additional voltage and current sensors are obligatory for each DC–DC converter. These additional sensors further increase the system complexity [9–11].

In single-phase multi-level inverters, the most widely used techniques are cascaded H-bridge (CHB), diode-clamped and capacitor-clamped types [12–15]. In addition, many other techniques also exist [8, 9, 11, 16–31]. In particular, among these techniques, CHB single-phase inverters have drawn attention because of their modularised circuit layout and simplicity [13, 32–38]. A variety of modulation techniques can be applied to CHB inverters. By increasing the number of CHBs, the number of levels in CHB inverters increases. Generally if the number of output voltage levels is increased, then the number of power electronic devices and the number of isolated DC sources is also increased. This makes a CHB inverter further complex.

In this paper, a multilevel inverter with minimum number of power electronic switching devices is proposed which is a modified version of the multilevel inverter using series/parallel conversion of DC sources (MLISPC) developed in [8]. In the proposed multilevel inverter, an auxiliary circuit comprising of four diodes and a switch is introduced instead of series/parallel switches of the inverter found in MLISPC. However, only two isolated voltage sources are needed to output the same number of voltage levels compared to conventional CHB inverters and MLISPC.

The number of switching devices used and the harmonics of the output voltage waveform for the proposed inverter are reduced as well when compared to the methods detailed above. The proposed multilevel inverter topology can be extended for the application of grid connected PV systems, hybrid electric vehicles etc. Furthermore, theoretical analysis, numerical simulations and experimental results are

also presented to demonstrate the validity of the proposed single-phase cascaded multilevel inverter.

Section 2 describes the circuit topology of the proposed multilevel inverter. In Section 3, the generalised pulse with modulation (PWM) modulation technique of the proposed inverter is explained. In Section 4, converter losses are discussed. In Section 5 the simulation and experimental results are validated.

2 Circuit topology

Fig. 1 shows the circuit configuration of the proposed cascaded H bridge multilevel inverter with two H bridge inverters connected in cascade (upper and lower H bridge inverters). Capacitor sources $v_{dc1} - v_{dcn}$ may either be independent or dependent on each other. The magnitude of each voltage sources in the lower H bridge is two times the magnitude of upper H bridge voltage source (i.e. $(v_{dcn}/v_{dc0}) = 2$). The lower H bridge of MLISPC is replaced with the one developed in [9, 17–19]. As shown in Fig. 1, in the lower H bridge, an auxiliary circuit comprising of four diodes and a switch is placed between two DC sources.

Using this proposed circuit configuration, the lower H bridge inverter outputs $V_{low} = 2n + 1$ levels, whereas the upper H bridge outputs $V_{up} = v_{dc0}$. The proposed inverter outputs $4n + 3$ levels by $V_{low} + V_{up}$ or $V_{low} - V_{up}$. Here, n is the number of capacitor sources in the lower H bridge inverter. Fig. 2 shows the lower H bridge inverter with two capacitor sources, which outputs five levels. The switching states of the five-level inverter (lower H bridge) are shown in Table 1.

Table 2 gives the complete switching states and the derived output of the proposed multilevel inverter to generate 11 levels. The modes of operation indicated in Table 2 correspond to the modes pointed out in Fig. 3. In Table 2, the symbol ↔ indicates that the voltage level switches between two extremes.

2.1 Capacitor voltage balancing

Since the main application of the proposed inverter is fed from PV array or FC stacks, DC–DC boost converters are required to boost the low output voltage of the PV panels or FC stacks. Hence here two boost converters are used, one for the upper H bridge inverter and another for the lower H bridge inverter. For the lower inverter a multioutput boost (MOB) DC–DC converter is used which is proposed in [20–22]. One of the most interesting

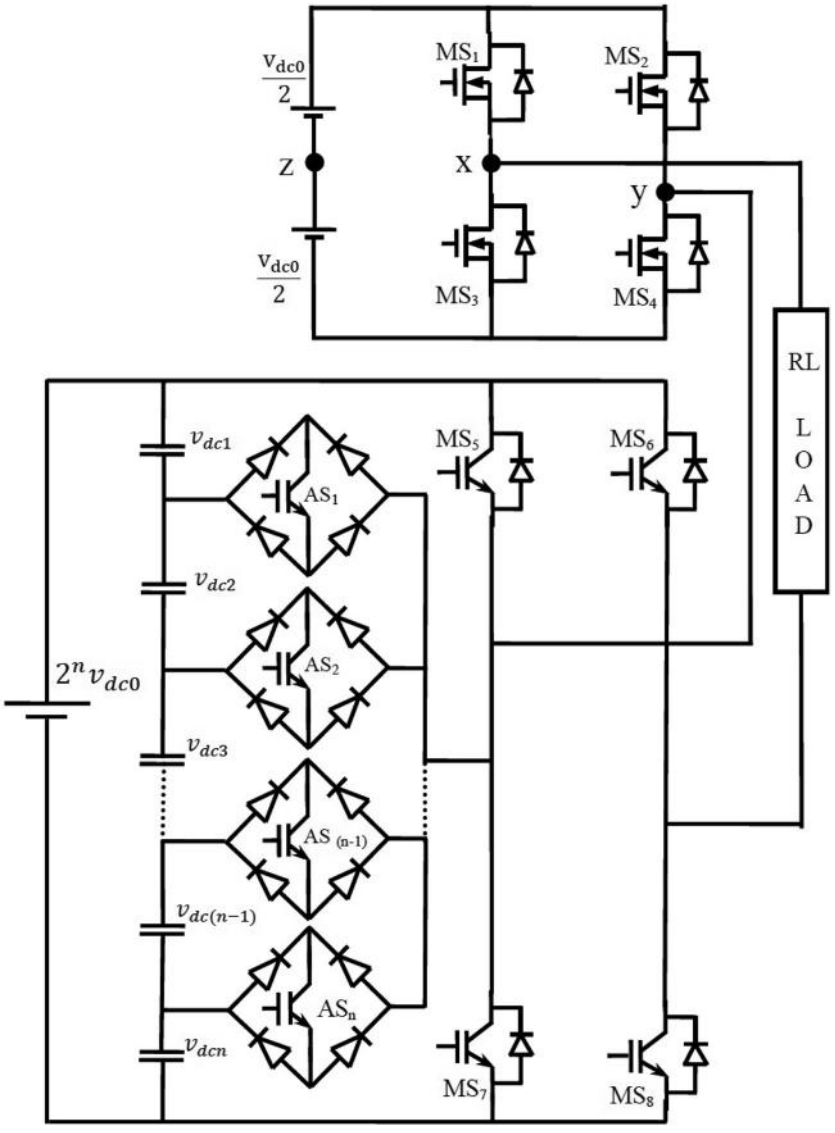

Fig. 1 *Proposed cascaded H bridge multilevel inverter*

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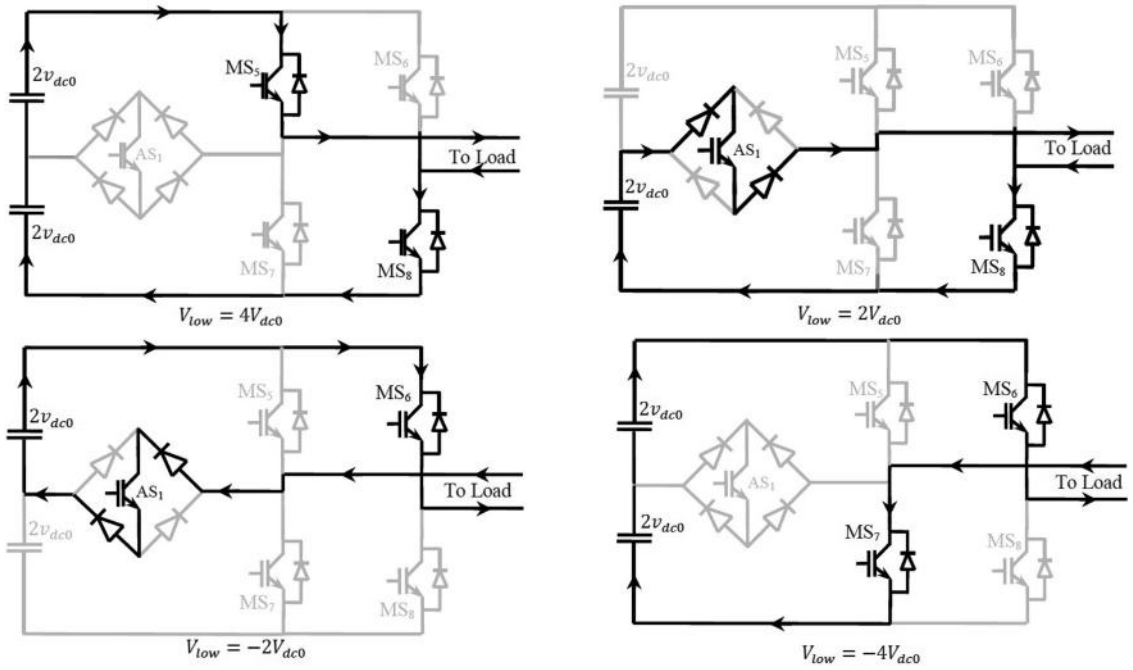

Fig. 2 *Operation of lower inverter*

Table 1 Switching states of lower H bridge inverter

V_{low}	MS_5	MS_6	MS_7	MS_8	AS_1	Reference
$4V_{dc}$	ON	OFF	OFF	ON	OFF	Fig. 2*a*
$2V_{dc}$	OFF	OFF	OFF	ON	ON	Fig. 2*b*
$-2V_{dc}$	OFF	ON	OFF	OFF	ON	Fig. 2*c*
$-4V_{dc}$	OFF	ON	ON	OFF	OFF	Fig. 2*d*

applications of this MOB DC–DC converter is the boosting and regulating the low and variable output voltage of renewable energy for the DC link of grid connected systems, based on multilevel inverters [21]. Hence the MOB DC–DC converter serves for two purposes, they are

1. for boosting low output voltage of PV array or FC stacks to a desired value;
2. balancing of DC link capacitors.

The schematic of the proposed inverter fed from multi-output DC–DC converter is shown in Fig. 4.

3 Generalised PWM modulation technique

This section determines the switching function to obtain a output of 11 levels in the proposed inverter. The same procedure can be extended to derive the switching function of N-level inverter. A hybrid PWM modulation technique is used to generate the PWM switching signals [24].

Fig. 5 shows the PWM modulation scheme of the proposed 11-level inverter. The total reference waveform is generated as shown in Fig. 3*a* and defined in

$$U_{\text{ref}} = A \sin(\omega t) \tag{1}$$

where A is the peak value of the reference waveform and is given by $2n+1$. The above equation is scaled down as given in

$$U_{\text{ref},S} = \frac{U_{\text{ref}}}{5} \tag{2}$$

The reference waveform for the upper inverter is generated by using the following expressions

Table 2 Switching states of proposed inverter

Upper inverter switches (high-frequency switches)				Lower inverter switches (low-frequency switches)					Derived output voltage $V_{dc1} = V_{dc2} = 2V_{dc0}$			Mode
MS_1	MS_2	MS_3	MS_4	MS_5	MS_6	MS_7	MS_8	AS_1	V_{up}	V_{low}	V_{total}	
ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	$0 \leftrightarrow V_{dc0}$	$4V_{dc0}$	$4V_{dc0} \leftrightarrow 5V_{dc0}$	I
OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	$-V_{dc0} \leftrightarrow 0$	$4V_{dc0}$	$3V_{dc0} \leftrightarrow 4V_{dc0}$	II
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	$0 \leftrightarrow V_{dc0}$	$2V_{dc0}$	$2V_{dc0} \leftrightarrow 3V_{dc0}$	III
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	$-V_{dc0} \leftrightarrow 0$	$2V_{dc0}$	$V_{dc0} \leftrightarrow 2V_{dc0}$	IV
ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	$0 \leftrightarrow V_{dc0}$	0	$0 \leftrightarrow V_{dc0}$	V
OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	$0 \leftrightarrow -V_{dc0}$	0	$0 \leftrightarrow -V_{dc0}$	VI
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	$V_{dc0} \leftrightarrow 0$	$-2V_{dc0}$	$-V_{dc0} \leftrightarrow -2V_{dc0}$	VII
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	$0 \leftrightarrow -V_{dc0}$	$-2V_{dc0}$	$-2V_{dc0} \leftrightarrow -3V_{dc0}$	VIII
ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	$V_{dc0} \leftrightarrow 0$	$-4V_{dc0}$	$-3V_{dc0} \leftrightarrow -4V_{dc0}$	IX
OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	$0 \leftrightarrow -V_{dc0}$	$-4V_{dc0}$	$-4V_{dc0} \leftrightarrow -5V_{dc0}$	X

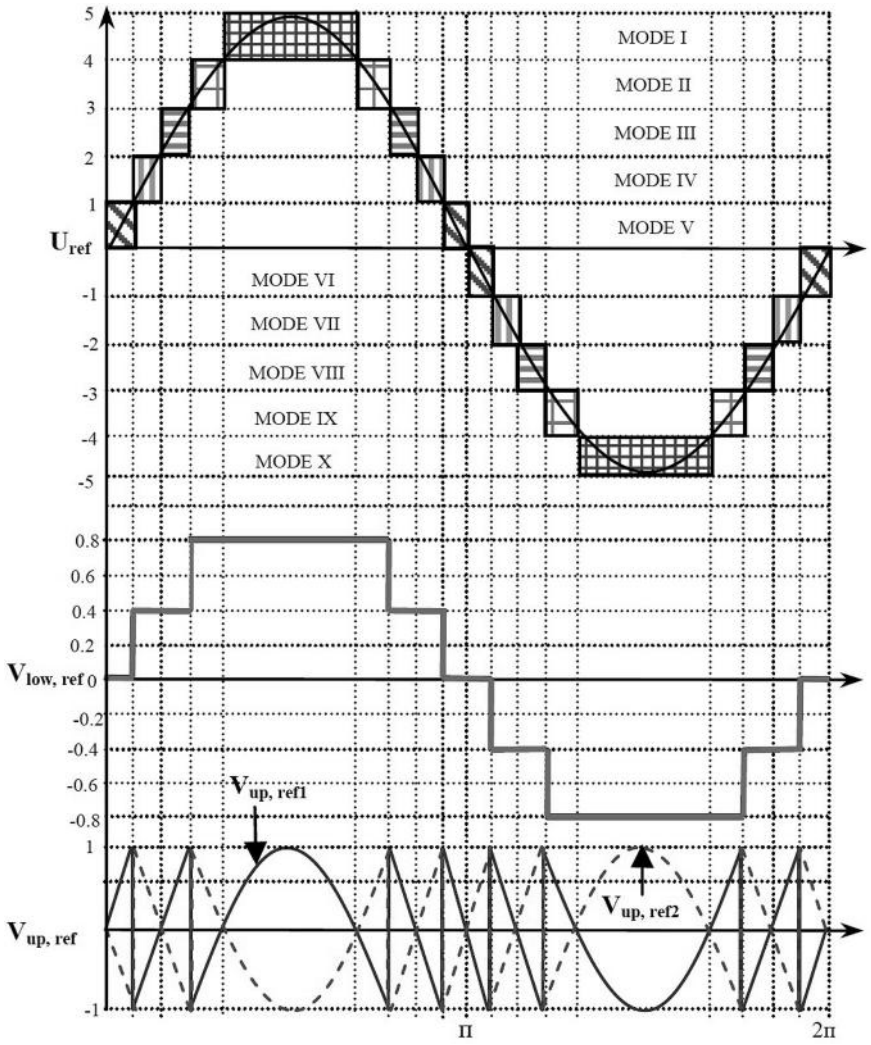

Fig. 3 *Reference waveform generation for upper bridge of 11-level inverter*

$$Z_1 = \begin{cases} 1 & \text{if } U_{\text{ref}} > 0 \\ 0 & \text{if } U_{\text{ref}} < 0 \end{cases} \tag{3}$$

$$V_{\text{Low,expected}} = \left(\text{round}\left(\frac{|U_{\text{ref},S}|}{0.4}\right) * 0.4 * Z_1\right) + \left(\text{round}\left(\frac{|U_{\text{ref},S}|}{-0.4}\right) * 0.4 * \bar{Z}_1\right) \tag{4}$$

$$V_{\text{UP,ref}} = 5 * \left(U_{\text{ref},S} - V_{\text{Low,expected}}\right) \tag{5}$$

Equation (3) is a simple zero crossing detector, whereas (4) gives the expected output of the lower H bridge inverter (v_{low}) and (5) is the mathematical representation of the upper H bridge inverter reference waveform. The output of (4) and (5) for 11-level inverter is shown in Figs. 3*b* and *c*. The above equations can be used for higher inverter levels by simply changing the value of A. For example, $A = 7$ for 15, $A = 9$ for 19 levels, $A = 11$ for 23 levels and so on can be obtained. In order to generate switching patterns for the lower inverter, the first step is to generate the reference waveform for the lower inverter

$$V_{\text{Low,ref}} = \text{round}\left(\frac{|U_{\text{ref},S}|}{0.4}\right) \tag{6}$$

The next step is to split the above reference wave into many signals of R_y

$$X = \frac{(N-11)}{4} + 2, \quad \text{where } N = 11, 15, 19, 23, \ldots \tag{7}$$

$$R_y = \begin{cases} 1 & \text{if } V_{\text{Low,ref}} > y \\ 0 & \text{if } V_{\text{Low,ref}} < y \end{cases} \tag{8}$$

where $y = 1$ to X. After dividing the reference of the lower inverter into many subsignals, it is necessary to find out the number of auxiliary switches required for an N-level inverter

$$\text{NAS} = \frac{(N-11)}{4} + 1, \quad \text{where } N = 11, 15, 19, 23, \ldots \tag{9}$$

The main switches of the lower inverter are switched as per the equations given below

$$\text{MS}_5(t) = \left[(\bar{R}_1) + (R_y)\right] * (Z_1) \tag{10}$$

$$\text{MS}_6(t) = \left[(R_1) * (\bar{Z}_1)\right] + \left[(\bar{R}_1) * (Z_1)\right] \tag{11}$$

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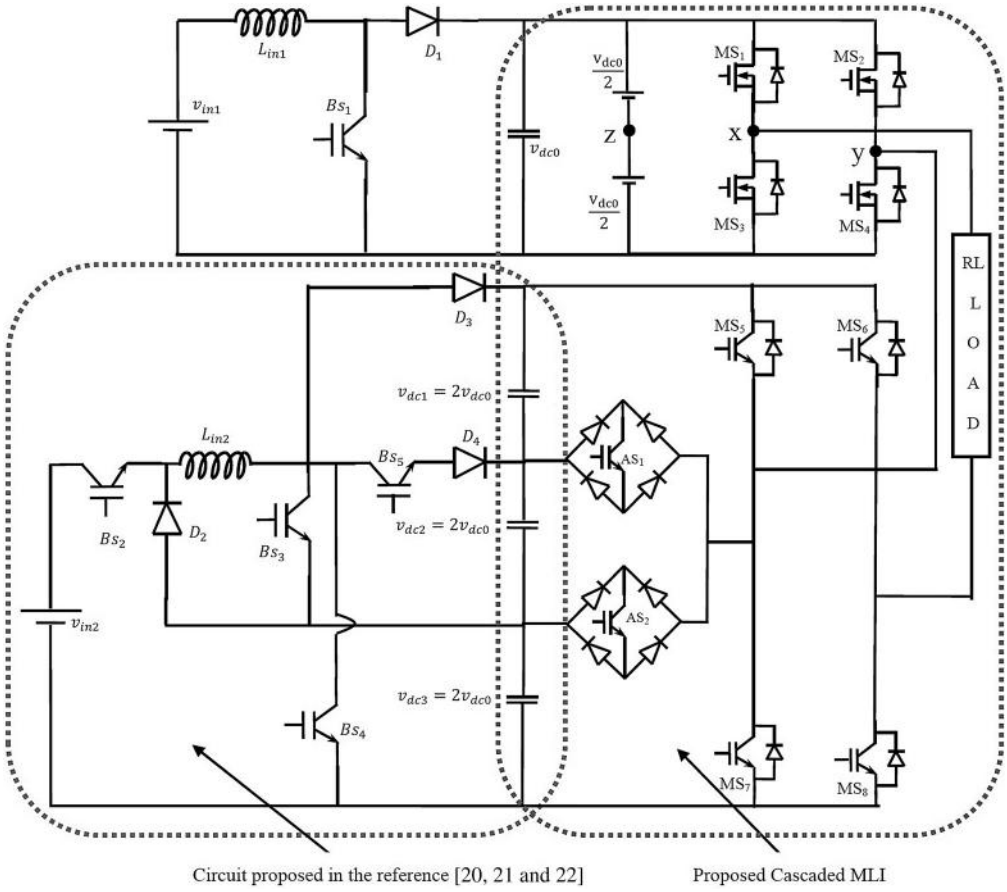

Fig. 4 *Proposed inverter fed from multioutput boost converter*

$$\mathrm{MS}_7(t) = \left[(\bar{R}_1) + (R_y)\right] * (\bar{Z}_1) \tag{12}$$

$$\mathrm{MS}_8(t) = \left[(R_1) * (Z_1)\right] + \left[(\bar{R}_1) * (\bar{Z}_1)\right] \tag{13}$$

where $y = X, +$ denotes logical OR operation and * denotes multiplication of signals. The auxiliary switches of the lower inverter can be switched as per the algorithm given below.

Step 1: Form a set

$$R = \left[R_1, R_2, R_3, R_4, \ldots, R_{y-3}, R_{y-2}, R_{y-1}, R_y\right] \tag{14}$$

Step 2: Write the permutation P on R as given below

$$P = \begin{bmatrix} R_1 & R_2 & R_3 & \ldots & R_{y-2} & R_{y-1} & R_y \\ R_2 & R_3 & R_4 & \ldots & R_{y-1} & R_y & R_1 \end{bmatrix} \tag{15}$$

Step 3: Remove the last column in the above permutation P_1 and rewrite as

$$P_1 = \begin{bmatrix} R_1 & R_2 & R_3 & \ldots & R_{y-3} & R_{y-2} & R_{y-1} \\ R_2 & R_3 & R_4 & \ldots & R_{y-2} & R_{y-1} & R_y \end{bmatrix} \tag{16}$$

Step 4: From the above equation, it is very easy to derive the switching pulses for all the auxiliary switches of the N level inverter. The first and last columns of the above matrix are responsible for developing switching patterns for first and last auxiliary switches and the equations for AS_1 and AS_n are

$$\mathrm{AS}_1(t) = \left((R_1 \oplus R_2) * \bar{Z}_1\right) + \left(\left(R_{y-1} \oplus R_y\right) * Z_1\right) \tag{17}$$

$$\mathrm{AS}_n(t) = \left((R_1 \oplus R_2) * Z_1\right) + \left(\left(R_{y-1} \oplus R_y\right) * \bar{Z}_1\right) \tag{18}$$

where $\oplus$ denotes XOR operation. Similarly, the second column from the first and second column from the last are responsible for developing switching patterns of AS_2 and $\mathrm{AS}_{(n-1)}$ and the equations are as given below

$$\mathrm{AS}_2(t) = \left((R_2 \oplus R_3) * \bar{Z}_1\right) + \left(\left(R_{y-2} \oplus R_{y-1}\right) * Z_1\right) \tag{19}$$

$$\mathrm{AS}_{n-1}(t) = \left((R_2 \oplus R_3) * Z_1\right) + \left(\left(R_{y-2} \oplus R_{y-1}\right) * \bar{Z}_1\right) \tag{20}$$

The above procedure can be repeated to generate switching patterns for any pair of auxiliary switches based on the following cases.

Case I (If P_1 contains odd number of columns): Some times as in the case of 19-level inverter, when $X = 4$, the number of R signals available will be four that is R_1, R_2, R_3 and R_4. Number of auxiliary switches in 19-level inverter will be three. As per the algorithm, the permutation P_1 will be

$$P_1 = \begin{bmatrix} R_1 & R_2 & R_3 \\ R_2 & R_3 & R_4 \end{bmatrix} \tag{21}$$

The first and last columns of the above P_1 will be responsible for constructing switching patterns for AS_1 and AS_3, but for

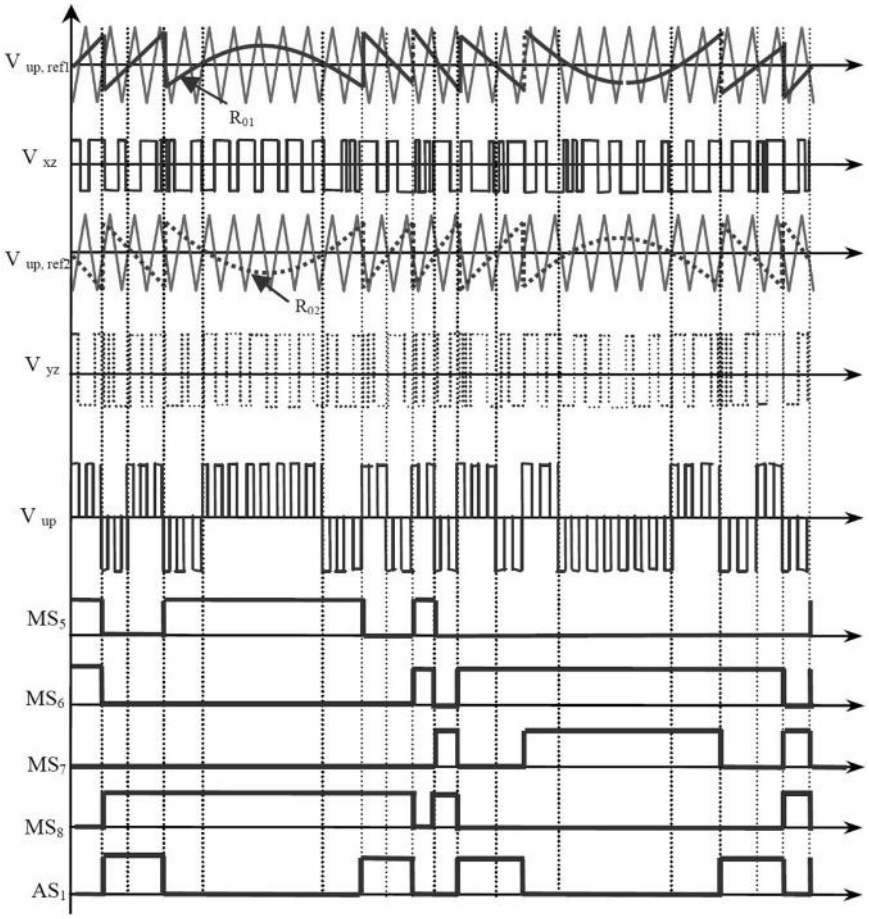

Fig. 5 *Modulation strategy of the proposed inverter*

developing the switching pattern for AS_2 only the centre column of the permutation P_1 should be used. Switching pattern for AS_2 can be developed as

$$AS_2(t) = (R_2 \oplus R_3) \tag{22}$$

The possibility of case I is also valid for $N = 11, 19, 27, 35, 43, \ldots$.

Case II (If P_1 contains even number of columns): As in 23-level inverter, when $X = 5$, the number of R signals available will be five that is R_1, R_2, R_3, R_4 and R_5 where as the number of auxiliary switches in 23-level inverter will be four. As per the algorithm, permutation P_1 will be

$$P_1 = \begin{bmatrix} R_1 & R_2 & R_3 & R_4 \\ R_2 & R_3 & R_4 & R_5 \end{bmatrix} \tag{23}$$

The first and last columns of the above P_1 will be responsible for constructing switching patterns for AS_1 and AS_4 and second and third columns are used for developing switching pattern for AS_2 and AS_3. As second and third columns have only three unique R signals that is R_2, R_3 and R_4, to develop switching patterns for AS_2 and AS_3 the following equations are used

$$AS_2(t) = \left((R_2 \oplus R_3) * \bar{Z}_1\right) + \left((R_3 \oplus R_4) * Z_1\right) \tag{24}$$

$$AS_3(t) = \left((R_2 \oplus R_3) * Z_1\right) + \left((R_3 \oplus R_4) * \bar{Z}_1\right) \tag{25}$$

The possibility of case II is also valid for $N = 15, 23, 31, 39, 47$ etc.

The modulation index M_a of the proposed N-level inverter is defined as

$$M_a = \frac{A_{\mathrm{pr}}}{MA_{\mathrm{pc}}} \tag{26}$$

where $M = (N - 1/2)$, $N = 11, 15, 19, 23, \ldots$ etc.

Where A_{Pr} represents the peak value of the modulating or reference wave and A_{pc} represents the peak-to-peak value of the carrier (triangular) wave. Main switches MS_1 and MS_3 are switched by comparing the reference waveform R_{01} with the carrier wave and as a result, voltage V_{xz} between points x and z in Fig. 1 appears as shown in Fig. 5. Main switches MS_2 and MS_4 are switched by comparing the reference waveform R_{02} with carrier wave and as a result, voltage V_{yz} between points y and z in Fig. 1 appears as shown in Fig. 3. Main switches of lower bridge inverter MS_5–MS_8 are switched as per (10)–(13) and auxiliary switch AS_1 is switched as per the proposed algorithm above as shown in Fig. 5. The proposed generalised algorithm is very simple since it makes use of simple logical operations.

4 Comparison of proposed inverter with other inverters

The proposed topology is compared with conventional symmetrical CHB inverters, MLISPC inverter, asymmetrical CHB inverter with 1:2:4 configuration and asymmetrical

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CHB inverter with 1:3:9 configuration. The comparison is done on the basis of converter losses and rating of the devices.

4.1 Converter losses

The average switching power loss P_{sloss} in the switch caused during the transition of switch is given by

$$P_{\text{sloss}} = \frac{1}{2} V_{\text{DS}} I_{\text{dc}} f_s \left(t_{\text{c(on)}} + t_{\text{c(off)}} \right) \tag{27}$$

where $t_{\text{c(on)}}$ and $t_{\text{c(off)}}$ are the turn-on and turn-off crossover intervals, respectively; V_{DS} is the voltage across the switch and I_{dc} is the current which flows through the switch. For more clarity, the proposed topology with 15 levels is compared with the familiar and similarly setup topologies. For simplification, the proposed topology and the well-known inverter topologies are assumed to be operated at same turn-on and turn-off crossover intervals and at the same I_{dc}. Then, the average switching power loss P_{sloss} is proportional to V_{DS} and f_s

$$P_{\text{sloss}} \propto V_{\text{DS}} f_s \tag{28}$$

The number of primary devices required for generating 15 levels in the proposed inverter is 10 and the voltage across these switches is V_{DC} for upper H bridge switches (4 numbers), $6V_{\text{DC}}$ for lower H bridge switches (4 numbers) and $4V_{\text{DC}}$ for auxiliary switches (2 numbers). The upper H bridge inverter switches at high frequency f_s, the lower H bridge inverter switches at fundamental frequency f_m and the auxiliary devices switch at two times the fundamental frequency ($2f_m$). Therefore the switching losses of the proposed inverter can be written as

$$\begin{aligned} P_{\text{sloss(Proposed)}} &= 4V_{\text{DC}} f_s + 4(6V_{\text{DC}}) f_m + 2(4V_{\text{DC}})(2f_m) \\ &= 4V_{\text{DC}} \left[f_s + 6f_m + 4f_m \right] \\ &= 4V_{\text{DC}} \left[f_s + 10f_m \right] \end{aligned} \tag{29}$$

Similarly, the number of primary devices required for generating 15 levels in MLISPC inverter is 14 and the voltage across these switches is V_{DC} for upper H bridge switches (4 numbers), $6V_{\text{DC}}$ for lower H bridge switches (4 numbers) and $2V_{\text{DC}}$ for series/parallel switches (6 numbers). The upper H bridge inverter switches at high frequency f_s, the lower H bridge inverter switches at fundamental frequency f_m and the series/parallel switches switch at two times the fundamental frequency ($2f_m$). Therefore the switching losses of the proposed inverter can be obtained as

$$\begin{aligned} P_{\text{sloss(MLISPC)}} &= 4V_{\text{DC}} f_s + 4(6V_{\text{DC}}) f_m + 6(2V_{\text{DC}})(2f_m) \\ &= 4V_{\text{DC}} \left[f_s + 6f_m + 6f_m \right] \\ &= 4V_{\text{DC}} \left[f_s + 12f_m \right] \end{aligned} \tag{30}$$

Likewise, for conventional symmetrical CHB inverters, the switching losses can be calculated as

$$P_{\text{sloss(symm,CHB)}} = 28V_{\text{DS}} f_s \tag{31}$$

For asymmetrical cascaded H bridge inverter with 1:2:4 configurations, the switching losses can be obtained as

$$P_{\text{sloss(asymm,CHB)}} = 28V_{\text{DS}} f_s \tag{32}$$

Since $f_s \gg f_m$ and from (27)–(32), among the various familiar

Table 3 Comparison of voltage rating of devices for various topologies of MLI

	Voltage ratings of the devices		
Topology	Upper H bridge	Lower H bridge	Intermediate H bridges
proposed topology	$\frac{1}{2n+1}\sum_{k=0}^{n} V_{\text{dc},k}$ for $(V_{\text{dc}n}/V_{\text{dc}0}) = 2$ and $\frac{1}{3n+1}\sum_{k=0}^{n} V_{\text{dc},k}$ for $(V_{\text{dc}n}/V_{\text{dc}0}) = 3$	main H bridge switches $= \sum_{k=1}^{n} V_{\text{dc},k}$ auxiliary switches $A_{s1} = A_{sn} = \left[\sum_{k=1}^{n} V_{\text{dc},k}\right]\left[\frac{n-1}{n}\right]$ $A_{s2} = A_{s,n-1} = \left[\sum_{k=1}^{n} V_{\text{dc},k}\right]\left[\frac{n-2}{n}\right]$ similarly, $A_{s3} = A_{s,n-2} = \left[\sum_{k=1}^{n} V_{\text{dc},k}\right]\left[\frac{n-3}{n}\right]$ and so on…	—
MLISPC	$\frac{1}{2n+1}\sum_{k=0}^{n} V_{\text{dc},k}$	main H bridge switches $= \sum_{k=1}^{n} V_{\text{dc},k}$ series parallel switches $\frac{2}{2n+1}\sum_{k=0}^{n} V_{\text{dc},k}$	—
conventional symmetrical CHB	$V_{\text{dc},1}$	$V_{\text{dc},1}$	$V_{\text{dc},1}$
asymmetrical CHB 1:2:4 configuration	$V_{\text{dc},}$	$4V_{\text{dc},1}$	$2V_{\text{dc},}$
asymmetrical CHB 1:3:9 configuration	$V_{\text{dc},}$	$9V_{\text{dc},1}$	$3V_{\text{dc},1}$

topologies, the proposed topology has minimum switching losses when compared to other topologies.

Since in the proposed inverter, at any point of time, the number of switches in conduction is only 4 (2 from the upper inverter and 2 from the lower inverter), therefore conduction losses P_{closs} of the proposed inverter is

$$P_{\text{closs}} = 4R_{\text{ON}}I^2 \tag{33}$$

where R_{ON} is the internal resistance of the switching device and I is the current flowing in the devices. Whereas, in the case of MLISPC topology, the number of conducting devices increases as the number of levels increase, which in turn, generally increases the conduction losses. The same is true for any well-known topologies. Hence, the conduction losses are less in the case of proposed topology when compared to MLISPC, conventional symmetrical CHB and asymmetrical CHB inverters. Further from (29) to (32), the switching lose is reduced by 3.8% when compared to the MLISPC and reduced by 82% when compared to the conventional asymmetrical cascaded H bridge inverter with 1:2:4 configurations.

4.2 Comparison based on voltage rating of the devices

The device rating of the switching devices should be selected sensibly in the proposed inverter, because the voltage rating of each device is different. In the 11-level topology of the proposed inverter, it requires only one auxiliary switch, in this case the auxiliary switch voltage will jump between 0 and (V_{dc}/2), where V_{dc} is the input DC source voltage of lower inverter. This is because total voltage of V_{dc} is divided into two by using two capacitors that is, (V_{dc}/2) each. Hence, the auxiliary switches have to block the capacitor voltage which is (V_{dc}/2). In 15-level inverter topology, it requires two auxiliary switches. The entire voltage V_{dc} will be divided into three-by-three capacitors that is, (V_{dc}/3) across each. So, the two auxiliary switches voltage will jump between 0 and ($2V_{\text{dc}}$/3). Further, in the case of 19-level inverter, it requires three auxiliary switches. The first and last auxiliary switch voltages will jump between 0 and ($3V_{\text{dc}}$/4) and the middle auxiliary switch voltage will jump between 0 and ($2V_{\text{dc}}$/4). Similarly, for other levels of inverters, the first and last auxiliary switch voltage jumps between 0 and (($n-1$)V_{dc}/n), whereas the other auxiliary switch voltage jumps between 0 and (($n-2$) V_{dc}/n), (($n-3$)V_{dc}/n)… and so on. Table 3 gives the comparison of voltage ratings of the devices for various topologies. From Table 3 it can be concluded that the voltage rating of the upper H bridge inverter switches and auxiliary switches in the lower H bridge inverter becomes smaller and smaller compared to the output voltage when the number of levels is increased.

Table 4 Simulation and experimental parameters

Parameter	Level 11	Level 15	Level 43
value of M	5	7	21
upper inverter voltage	65	47	15.5
lower inverter voltage	130	94	31
load resistance and inductance are $R_L = 100\ \Omega$ and $L_L = 30$ mH			
filter inductance and capacitance are $L_f = 1.5$ mH and $C_f = 12.5\ \mu$F			

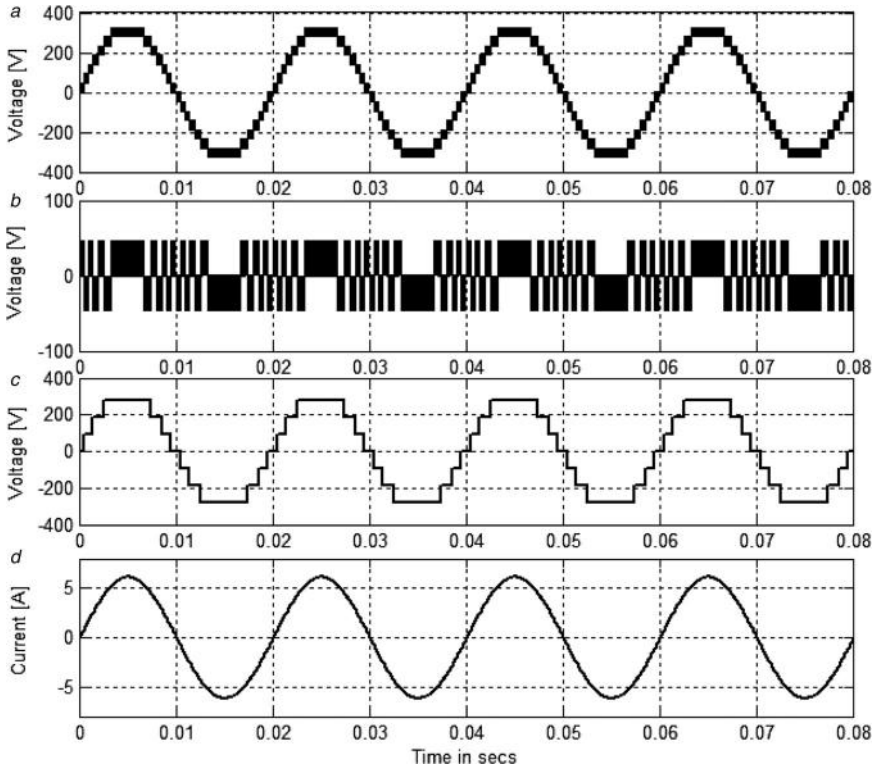

Fig. 6 *Simulated waveforms of a 15-level inverter along with upper and lower inverter waveforms for the modulation index of $M_a = 1$ (i.e. $A = 7$)*

a Voltage across the load (15 levels)
b Voltage across the upper inverter V_{up}
c Voltage across the lower inverter V_{low}
d Load current waveform for modulation index $M_a = 1$

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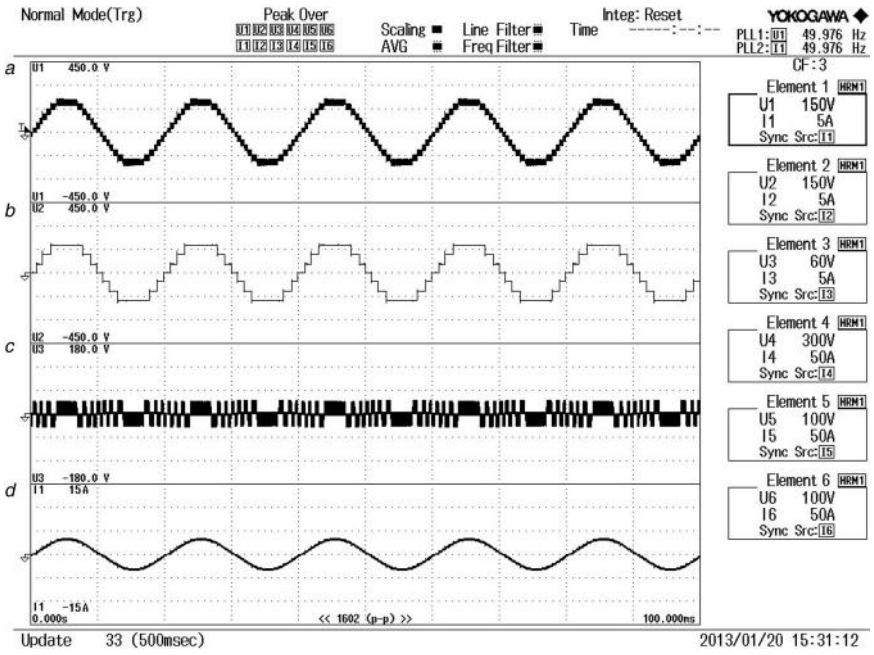

Fig. 7 *Hardware results when 15-level inverter is driven by $M_a = 1$*

a Voltage across the load
b Voltage across the lower inverter V_{low}
c Voltage across the upper inverter V_{up}
d Load current waveform

5 Simulation and experimental results

To validate the proposed inverter topology, simulation is carried out for the proposed inverter in Matlab/Simulink and the simulation results are verified experimentally. In the developed hardware prototype, the DC supply is given to the upper and lower inverter, by using separate DC–DC boost converters. The upper inverter is fed from a conventional

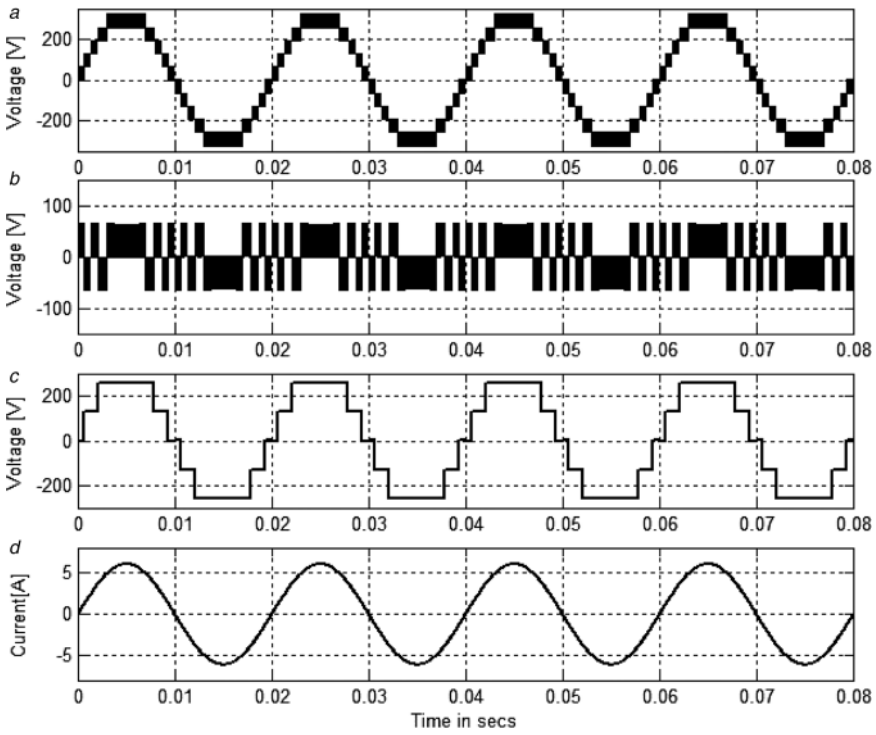

Fig. 8 *Simulation waveforms of 15-level inverter together with the upper and lower inverter voltages, when the modulation index is set to 0.7 (i.e. when the value of A = 5)*

a Voltage across the load (11 levels)
b Voltage across the upper inverter V_{up}
c Voltage across the lower inverter V_{low}
d Load current waveform for modulation index $M_a = 0.7$

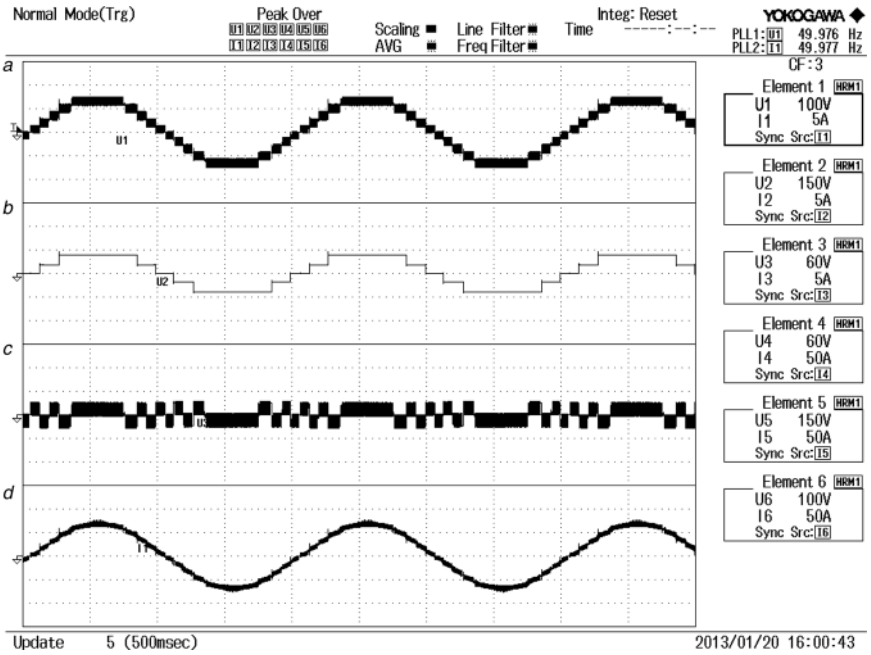

Fig. 9 *Hardware results when 15-level inverter is driven by $M_a = 0.7$*

a Voltage across the load (11 levels)
b Voltage across the lower inverter V_{low}
c Voltage across the upper inverter V_{up}
d Load current waveform

boost converter whereas the lower inverter is fed from a MOB converter proposed in [20]. The upper and lower inverter consists of MKI 80-06T6 K series insulated-gate bipolar transistors. The auxiliary switch used in the lower inverter is FIO50-12BD, a bidirectional device. The gate driving signal is developed by using field programmable gate array (FPGA)-Xilinx SPATRAN 3A DSP. The software used to develop programs for SPATRAN 3A DSP are Xilinx ISE Design Siute and Multisim. The conditions set for simulation and experiment are same. Table 4 gives the simulation and experimental parameters for 11-, 15- and 43-level inverters. The upper inverter is operated at high switching rate that is equivalent to the carrier frequency (i.e. 10 kHz), whereas the lower inverter is operated at low frequency (nearly equal to the fundamental frequency i.e. 50 Hz).

Fig. 6 shows the simulated waveforms of a 15-level inverter along with upper and lower inverter waveforms for the modulation index of $M_a = 1$ (i.e. $A = 7$). Fig. 7 shows the experimental results of 15-level inverter with modulation index of 1. Any decrease in the value of A further leads to reduce the output voltage level.

The algorithm discussed in Section 3 is implemented in the simulation up to 43 levels and the same can be extended to any required level.

Fig. 8 shows the simulation waveforms of 15-level inverter together with the upper and lower inverter voltages, when the

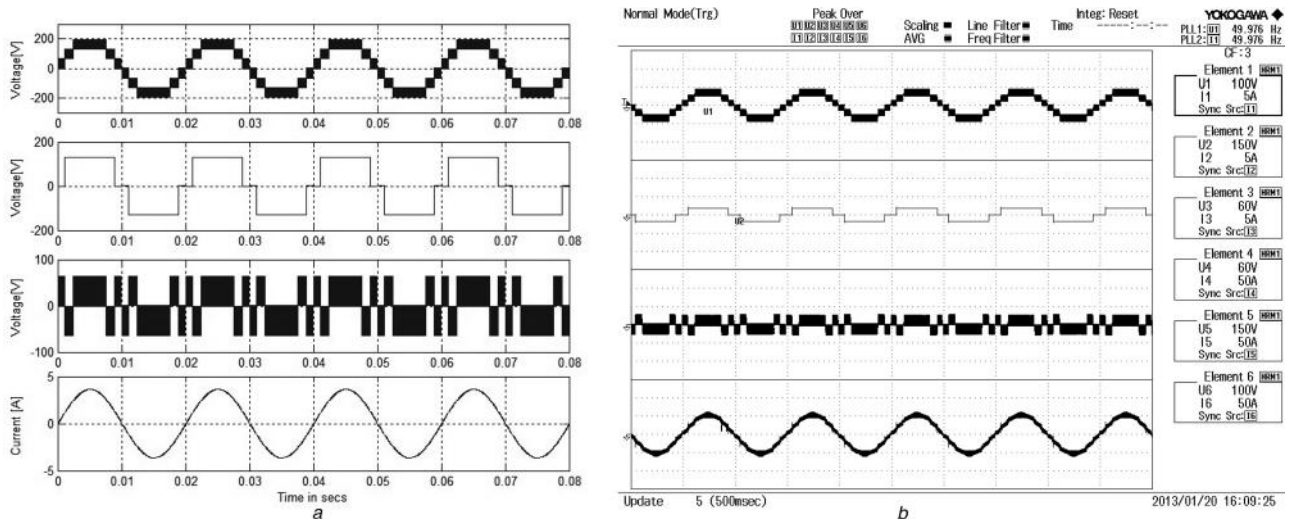

Fig. 10 *Voltage across the load, lower inverter, upper inverter and load current waveform when $M_a = 0.42$ (seven levels)*

a Simulation results
b Experimental results

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Table 5 Total harmonic distortion (THD) for voltage and current for various levels

		Voltage THD		Current THD	
Levels	*A*	WOF	WLCF	WOF	WLCF
43	21	2.67	0.03	1.83	0.87
15	7	7.98	0.06	4.98	1.06
13	6	9.21	0.03	6.34	1.82
11	5	11.27	0.09	8.09	2.32
9	4	14.34	0.03	10.57	4.29
7	3	18.91	0.20	12.45	4.89
5	2	28.86	0.05	18.79	5.67
3	1	56.7	0.80	20.28	8.53

WOF – without filter
WLCF – with LC filter

modulation index is set to 0.7 (i.e. when the value of $A = 5$). This reduces the number of levels at the load voltage from 15 to 11. To support the simulated waveforms, modulation index is set to 0.7 in the FPGA processor. Fig 9 shows the experimental waveforms of the proposed 15-level inverter when $M_a = 0.7$.

Fig. 10*a* shows the simulated waveform of the proposed 15-level inverter, when the modulation index is set to 0.42 (i.e. when the value of $A = 3$) resulting in 7 levels at the load terminals. Fig. 10 also shows simulated voltage waveform of the upper and lower inverters. The results of simulation are verified in the hardware setup by setting $M_a = 0.42$ in the FPGA processor as shown in Fig. 10*b*.

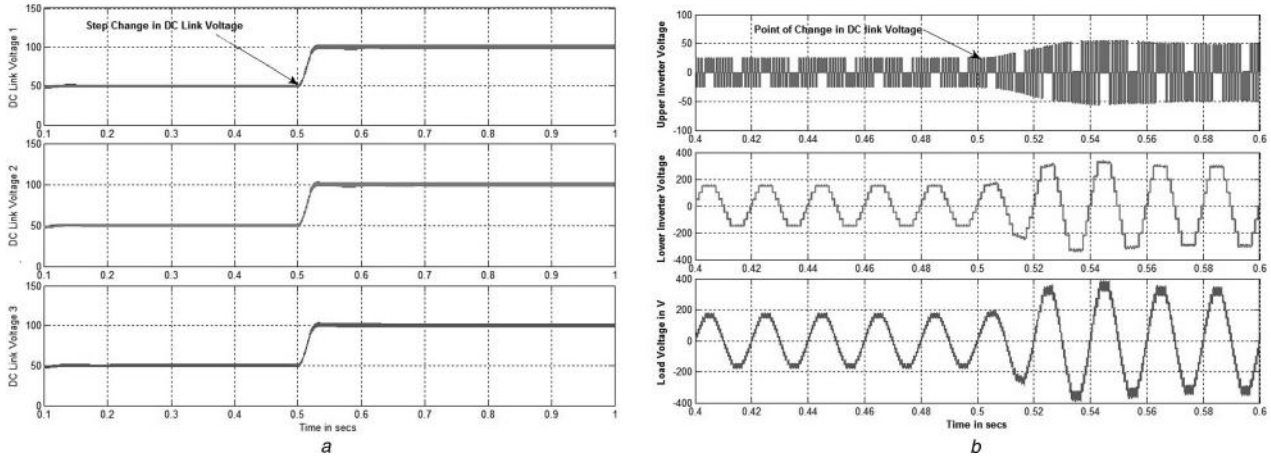

Fig. 11 *Dynamic response of the proposed inverter fed from MOB converter*

a DC link capacitor voltages of lower inverter
b Upper inverter, lower inverter and load voltage waveforms

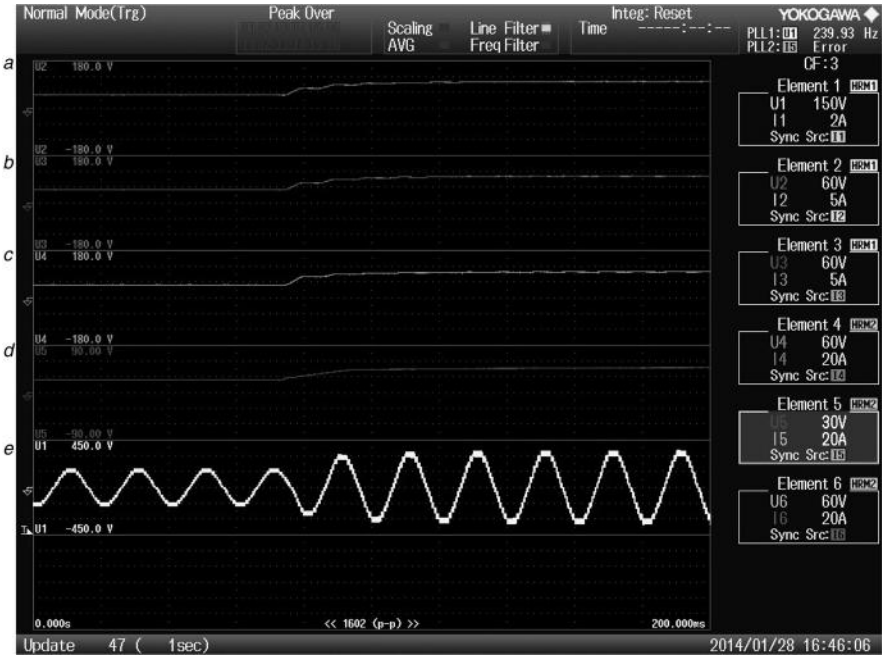

Fig. 12 *Experimental waveforms of the upper and lower capacitor voltages for step change in DC link voltages*

a, *b* and *c* Lower inverter DC link capacitor voltages
d Upper inverter DC link voltage
e Load voltage waveform

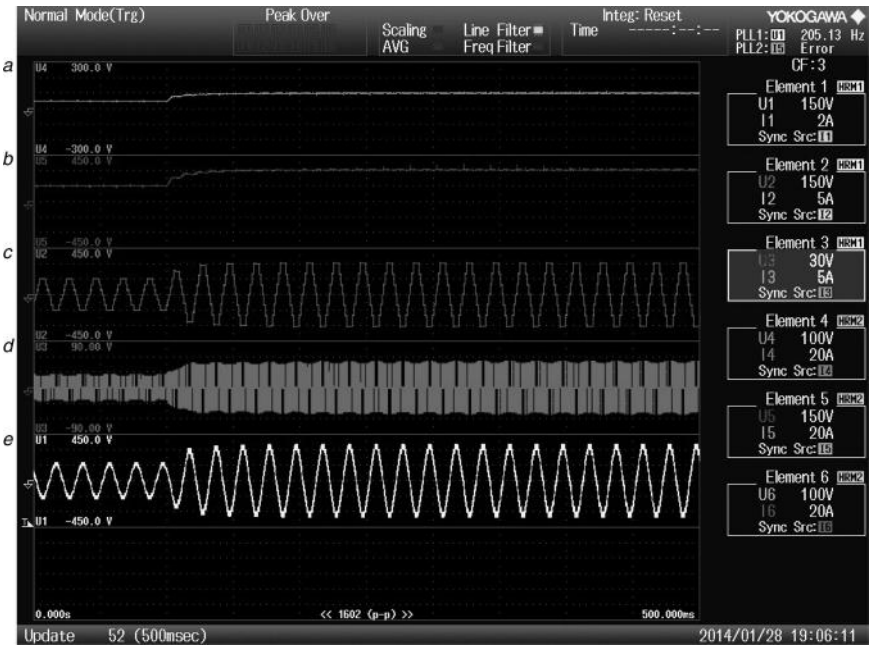

Fig. 13 *Dynamic response of upper and lower inverter voltages along with load voltage*

a Upper inverter DC link voltage
b Lower inverter DC link voltage
c Lower inverter voltage
d Upper inverter voltage
e Load voltage

Any reduction in the modulation index further will reduce the number of voltage levels at the load end. For example when $A = 2$ that is, $M_a = 0.28$, voltage level at the load becomes five and so on. Table 5 gives the details of total harmonic distortion at the load voltage and current for various output voltage levels.

In order to validate the proposed multilevel inverter fed from multioutput DC–DC boost converter, a step change in the reference values of the lower DC link capacitors were given at 0.5 s (i.e. from 50 to 100 V). Fig. 11*a* shows simulation results corresponding to the changes in the DC link capacitor voltages. Fig. 11*b* shows simulation results of the upper and lower inverter voltage along with load voltage response owing to step change in DC link capacitor voltages. Similarly a step change in the upper boost converter is given at 0.5 s (i.e. from 25 to 50 V) in order to

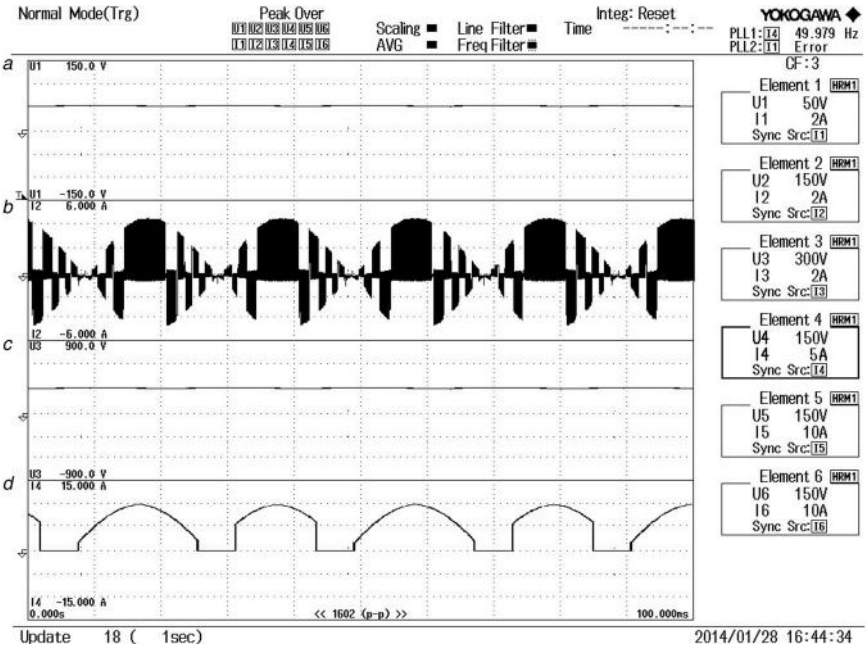

Fig. 14 *Experimental results*

a DC link voltage of upper inverter
b Current drawn from the upper inverter
c DC link voltage of lower inverter
d Current drawn from the lower inverter

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maintain the ratio between the lower and upper inverter DC link voltages as two. Fig. 12 shows the experimental waveforms of the upper and lower capacitor voltages owing to step change in their reference values (i.e. upper capacitor voltage is changed from 25 to 50 V and lower capacitor voltages are changed from 50 to 100 V). Fig. 13 shows the corresponding changes in the upper inverter and lower inverter voltages along with load voltage.

The voltage and current supplied by the upper and lower H bridge inverter is shown in Fig. 14. From Fig. 14 that nearly 90% of the power is controlled by the lower inverter. It can also be seen that the upper converter with small voltage only manages 10% of the total power. In real applications, since lower H bridge inverter is switched at the frequency close to the fundamental, it minimises switching losses and improves efficiency.

6 Conclusion

Multilevel inverters offer enhanced output waveforms with minimum THD. This paper has presents a novel single-phase multilevel inverter with reduced switching devices and isolated DC sources. Simulations are carried out in MATLAB/Simulink and implemented in real-time using FPGA board. A generalised switching algorithm that can be used for any number of levels is also presented. The performance of the suggested novel multilevel inverter is investigated in detail. The modulation waveform and the harmonic analysis are also presented for various values of modulation indices. By properly adjusting the modulation index, the required number of levels of the inverter output voltage can be achieved.

The simulation and experimental results match perfectly with each other. This proposed inverter system offers the advantage of reduced switching devices and isolated DC sources when compared to the conventional CHB and MLISCP for the same number of output levels. Also, high-frequency switching devices are operated at low voltage and low-frequency devices are operated at high voltage. Thus, it can be concluded that the proposed novel multilevel inverter can be used for medium- and high-power applications.

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