JPE 14-3-10

http://dx.doi.org/10.6113/JPE.2014.14.3.507
ISSN(Print): 1598-2092 / ISSN(Online): 2093-4718

Experimental Validation of a Cascaded Single Phase H-Bridge Inverter with a Simplified Switching Algorithm

Kaliamoorthy Mylsamy[†], Rajasekaran Vairamani[*], Gerald Christopher Raj Irudayaraj[*], and Hubert Tony Raj Lawrence[**]

[†*]Dept. of Electrical and Electronics Eng., PSNA College of Engineering and Technology, Dindigul, India
[**]Dept. of Electrical and Electronics Eng., Christian College of Engineering and Technology, Ottanchatriam, India

Abstract

This paper presents a new cascaded asymmetrical single phase multilevel converter with a lower number of power semiconductor switches and isolated DC sources. Therefore, the number of power electronic devices, converter losses, size, and cost are reduced. The proposed multilevel converter topology consists of two H-bridges connected in cascaded configuration. One H-bridge operates at a high frequency (high frequency inverter) and is capable of developing a two level output while the other H-bridge operates at the fundamental frequency (low frequency inverter) and is capable of developing a multilevel output. The addition of each power electronic switch to the low frequency inverter increases the number of levels by four. This paper also introduces a hybrid switching algorithm which uses very simple arithmetic and logical operations. The simplified hybrid switching algorithm is generalized for any number of levels. The proposed simplified switching algorithm is developed using a TMS320F2812 DSP board. The operation and performance of the proposed multilevel converter are verified by simulations using MATLAB/SIMULINK and experimental results.

Key words: Cascaded H-Bridge (CHB), Generalized hybrid modulation switching strategy, Hybrid multilevel inverter

I. INTRODUCTION

In recent years, the demand for green energy has been heading towards a huge distribution of electric generators driven by solar, wind, fuel cell, hydro, and other renewable energy sources. This tendency will extend throughout the subsequent years because the power produced by renewable sources is expected to satisfy 30% and 60% of the comprehensive needs in the years 2020 and 2050, respectively.

An important consequence of this circumstance is the need to replace the present electric power system, which consists of a low number of very high power ac generators, to a scattered one, which has a huge number of small to medium power ac and dc generators supplied by renewable energy sources connected to the grid through power electronic converters.

Manuscript received Nov. 13, 2013; accepted Feb. 17, 2014
Recommended for publication by Associate Editor Rae-Young Kim.
[†]Corresponding Author:kalias_ifet@yahoo.com
Tel: +919865065166, ., PSNA College of Engineering and Tech.
[*]Dept. of Electrical and Electronics Eng., PSNA College of Engineering and Technology, India
[**]Dept. of Electrical and Electronics Eng., Christian College of Engineering and Technology, India

This new development introduces various political, financial, and technical challenges because it alters the way in which the electrical energy resources (generation, transmission and distribution) are designed and controlled. From the technical perspective, the use of power electronic converters creates new issues, including increased complexity, increased power losses, electromagnetic interferences (EMIs) and reduced power quality, thus reducing the overall efficiency and stability.

Hence, numerous researchers have put their efforts in proposing new inverter configurations or in altering the existing ones, to improve the quality of the power available at the inverter terminals. Among the various inverter topologies, pulse width modulated (PWM) multilevel inverters (MLIs) are very popular [1]. In the beginning, they were used mainly in high-voltage high-power applications since the applied voltage is distributed among a number of cascaded power devices, thus overcoming their voltage limits [2]-[7]. As their output voltage is staircase in nature, they are better than two-level PWM inverters in terms of total harmonic distortion (THD), without the use of hefty, costly and dissipative passive filters. Therefore, in recent times, MLIs have been recommended in the field of renewable energies, including photovoltaic (PV) and fuel cell

(FC) generators [8]-[10].

There are three fundamental MLI configurations: neutral point clamped, flying capacitor MLIs, and cascaded H-bridge MLIs (CHB-MLI). The neutral point clamped and flying capacitor MLIs require only one DC source to develop a multilevel output whereas the CHB-MLI requires more than one isolated DC source. The CHB-MLI cannot be used when a single dc source is available. However, this drawback becomes a very attractive feature in the case of PV or FC systems, because solar cells or fuel cell stacks can be assembled in a number of separate generators.

A significant problem in multilevel converter design is the complexity of their control and pulse width modulator. Many authors have proposed diverse solutions (e.g., [11]-[35]). Generally if the number of output voltage levels is increased, then the number of power electronic devices and the number of isolated DC sources are also increased. This makes a CHB inverter even more complex.

In the case of the converters for PV and FC generators, another important issue is the achievement of maximum power point tracking (MPPT). DC-DC converters are mandatory for each of the isolated DC sources in a PV or FC application. These converters adjust the variable or low quality output voltage of PV or FC stacks. In addition, the power output of PV and FC stacks has to be maximized as it depends on ecological factors. Therefore, in order to track the maximum power point of the photovoltaic string or fuel cell stacks, additional voltage and current sensors are required for each DC-DC converter. These additional sensors further increase the system complexity.

In this paper, a multilevel inverter with a minimum number of power electronic switching devices is proposed. It is a modified version of a multilevel inverter using the series/parallel conversion of DC sources (MLISPC) developed in [15]. In the proposed multilevel inverter, an auxiliary circuit comprising of four diodes and a switch is introduced instead of the series/parallel switches of the inverter found in the MLISPC. However, only two isolated voltage sources are needed to output the same number of voltage levels when compared to conventional CHB inverters and the MLISPC.

The number of switching devices used and the harmonics of the output voltage waveform for the proposed inverter are reduced when compared to the conventional methods. The proposed multilevel inverter topology can be extended for the application of grid connected photo voltaic systems, hybrid electric vehicles, etc. Theoretical analysis, numerical simulations and experimental results are presented to demonstrate the validity of the proposed cascaded asymmetrical single phase multilevel converter.

Section II describes the circuit topology of the proposed multilevel inverter. In Section III, the generalized PWM modulation technique of the proposed inverter is explained. In Section IV, the converter losses are discussed. Sections V and VI validate the simulation and experimental results.

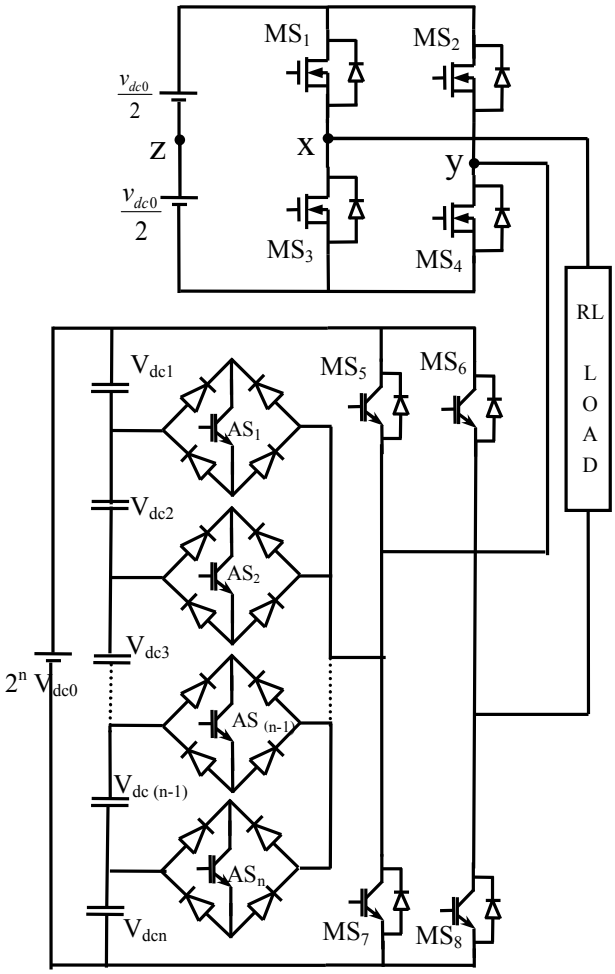
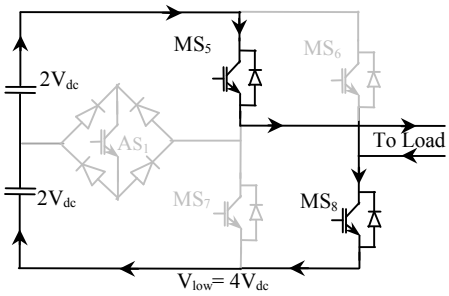


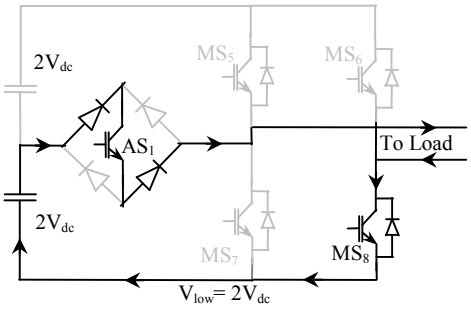
Fig. 1. Proposed cascaded H-bridge multilevel inverter.

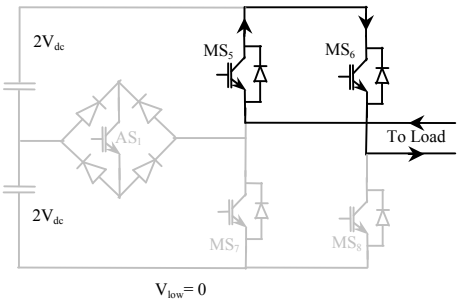
II. CIRCUIT TOPOLOGY

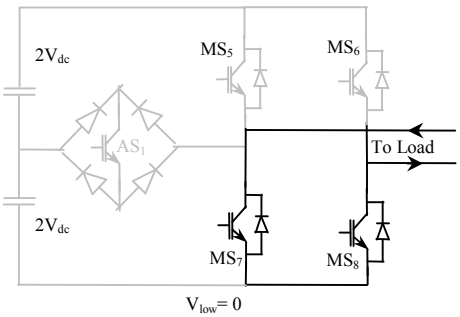
Fig. 1 shows the circuit configuration of the proposed cascaded H-bridge multilevel inverter with two H-bridge inverters connected in cascade (upper and lower H-bridge inverters). The DC voltage sources $v_{dco} - v_{dcn}$ may either be independent or dependent on each other. The magnitude of each voltage source in the lower H-bridge is two times the magnitude of the upper H-bridge voltage source (i.e. $v_{dcn} / v_{dc0} = 2$). The lower H-bridge of the MLISPC is replaced with the one developed in [13], [14], [16], [17]. As shown in Fig. 1, in the lower H-bridge, an auxiliary circuit comprising of four diodes and a switch placed between two DC sources.

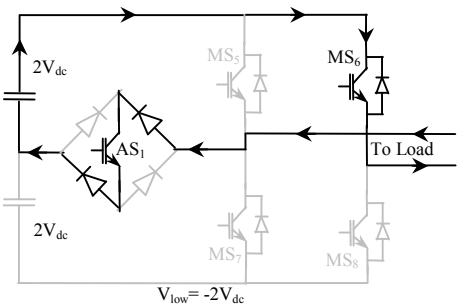
Using the proposed circuit configuration, the lower H-bridge inverter outputs V_{low} = 2n+1 levels, while the upper H-bridge outputs $V_{up} = v_{dc0}$. The proposed inverter outputs 4n + 3 levels by $V_{low} + V_{up}$ or V_{low}-V_{up}. Here, n is the number of capacitor sources in the lower H-bridge inverter. Fig. 2 shows the lower H-bridge inverter with two capacitor sources, which outputs











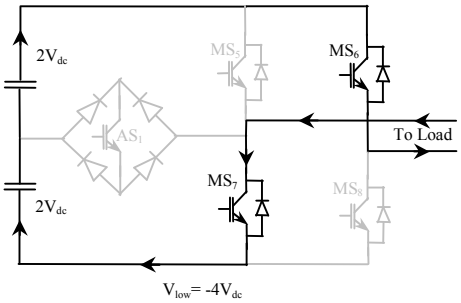


Fig. 2. Operation of lower inverter.

TABLE I

SWITCHING STATES OF LOWER H-BRIDGE INVERTER

V_{low}	MS_5	MS_6	MS_7	MS_8	AS_1	Reference
$4V_{dc}$	ON	OFF	OFF	ON	OFF	Fig 2(a)
$2V_{dc}$	OFF	OFF	OFF	ON	ON	Fig 2(b)
0	ON	ON	OFF	OFF	OFF	Fig 2(c)
0	OFF	OFF	ON	ON	OFF	Fig 2(d)
$-2V_{dc}$	OFF	ON	OFF	OFF	ON	Fig 2(e)
$-4V_{dc}$	OFF	ON	ON	OFF	OFF	Fig 2(f)

five levels. The switching states of the five level inverter (lower H-bridge) are shown in the Table I.

Table II gives the complete switching states and the derived output of the proposed multilevel inverter to generate 11 levels. The modes of operation indicated in Table II correspond to the modes pointed out in Fig. 4. In Table II, the symbol ↔ indicates that the voltage level switches between two extremes.

A. Capacitor Voltage Balancing

Since the main application of the proposed inverter is fed from a photovoltaic (PV) array or fuel cell (FC) stacks, DC-DC boost converters are required to boost the low output voltage of the PV panels or FC stacks. Hence, two boost converters are used, one for the upper H-bridge inverter and the other for the lower H-bridge inverter. For the lower inverter, the Multi Output Boost (MOB) DC-DC converter proposed in [36] is used. One of the most interesting applications of this MOB DC-DC converter is the boosting and regulation of the low and variable output voltage of renewable energy for the DC link of grid connected systems, based on multilevel inverters [2]. Hence, the MOB DC-DC converter serves the following two purposes:

1) Boosting the low output voltage of the PV array or FC stacks to a desired value.
2) Balancing of the DC link capacitors.

The proposed inverter, fed from a multi output DC-DC converter, is shown in Fig 5.

III. GENERALIZED PWM MODULATION TECHNIQUE

This section determines the switching function to get the

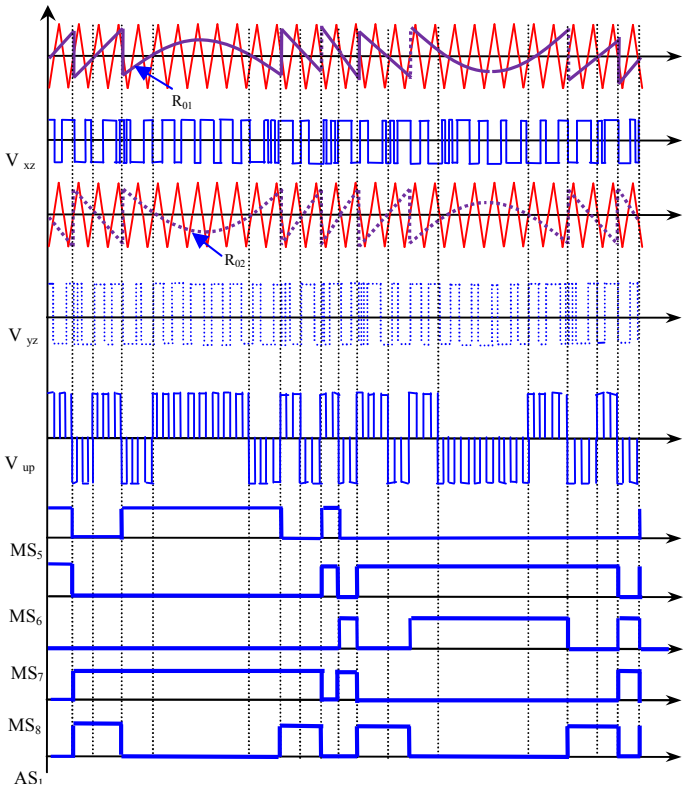


Fig. 3. Modulation strategy of the proposed inverter.

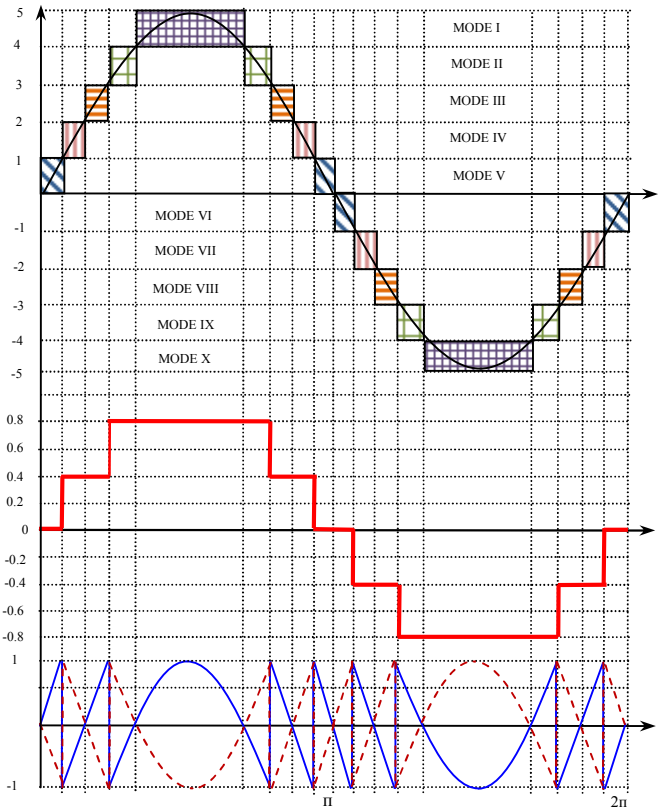


Fig. 4. Reference waveform generation for an 11 level inverter (upper bridge).

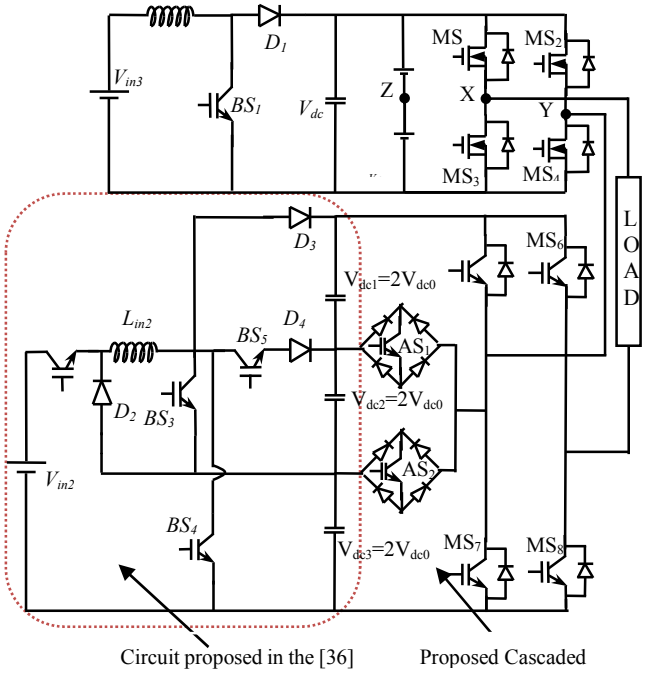


Fig. 5. Proposed cascaded H-Bridge multilevel inverter fed from multi output boost converter.

output of the eleven levels in the proposed inverter. The same procedure can be extended to derive the switching function of an N level inverter. A hybrid PWM modulation technique is used to generate the PWM switching signals [19]. Fig 3 shows the PWM Modulation scheme of the proposed 11 level inverter. The total reference waveform is generated as shown in Fig. 4 (a) and defined in (1).

$$U_{ref} = A \sin(\omega t) \tag{1}$$

Where A is the peak value of the reference waveform. (A = 5 for 11 level inverter). The above equation is scaled down as given in (2).

$$U_{ref,s} = \frac{U_{ref}}{5} \tag{2}$$

The reference waveform for the upper inverter is generated by using the following expressions:

$$Z_1 = \begin{cases} 1 & \text{if } U_{ref} > 0 \\ 0 & \text{if } U_{ref} < 0 \end{cases} \tag{3}$$

$$V_{Low,expected} = \left(round\left(\frac{|U_{ref,s}|}{0.4} \right) * 0.4 * Z_1 \right) + \left(round\left(\frac{|U_{ref,s}|}{-0.4} \right) * 0.4 * Z_1 \right) \tag{4}$$

$$V_{UP,ref} = 5 * \left(U_{ref,s} - V_{Low,expected} \right) \tag{5}$$

TABLE II
SWITCHING STATES OF PROPOSED INVERTER

Upper Inverter Switches (High Frequency Switches)				Lower Inverter Switches (Low Frequency Switches)					Mode	Derived output voltage $V_{dc1} = V_{dc2} = 2V_{dc0}$ $i.e$ $\left[\frac{V_{dcn}}{V_{dc0}} = 2\right]$		
MS_1	MS_2	MS_3	MS_4	MS_5	MS_6	MS_7	MS_8	AS_1		V_{up}	V_{low}	$V_{total} = V_{up} + V_{low}$
ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	I	$0 \leftrightarrow V_{dc0}$	$4V_{dc0}$	$4V_{dc0} \leftrightarrow 5V_{dc0}$
OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	II	$-V_{dc0} \leftrightarrow 0$	$4V_{dc0}$	$3V_{dc0} \leftrightarrow 4V_{dc0}$
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	III	$0 \leftrightarrow V_{dc0}$	$2V_{dc0}$	$2V_{dc0} \leftrightarrow 3V_{dc0}$
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	IV	$-V_{dc0} \leftrightarrow 0$	$2V_{dc0}$	$V_{dc0} \leftrightarrow 2V_{dc0}$
ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	V	$0 \leftrightarrow V_{dc0}$	0	$0 \leftrightarrow V_{dc0}$
OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	VI	$0 \leftrightarrow -V_{dc0}$	0	$0 \leftrightarrow -V_{dc0}$
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	VII	$V_{dc0} \leftrightarrow 0$	$-2V_{dc0}$	$-V_{dc0} \leftrightarrow -2V_{dc0}$
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	VIII	$0 \leftrightarrow -V_{dc0}$	$-2V_{dc0}$	$-2V_{dc0} \leftrightarrow -3V_{dc0}$
ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	IX	$V_{dc0} \leftrightarrow 0$	$-4V_{dc0}$	$-3V_{dc0} \leftrightarrow -4V_{dc0}$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	X	$0 \leftrightarrow -V_{dc0}$	$-4V_{dc0}$	$-4V_{dc0} \leftrightarrow -5V_{dc0}$

Equation (3) is a simple zero crossing detector, while (4) gives the expected output of the lower H-bridge inverter (Vlow) and (5) is a mathematical representation of the upper H-bridge inverter reference waveform. The output of equations (4) and (5) for the 11 level inverter are shown in Fig. 4(b) and Fig. 4(c). The above equations can be used for higher inverter levels by simply changing the value of A. For example, A = 7 for 15 levels, A = 9 for 19 levels, A = 11 for 23 levels just to mention a few. In order to generate the switching patterns for the lower inverter, the first step is to generate the reference waveform for the lower inverter.

$$V_{Low,ref} = round\left(\frac{\left|U_{ref,S}\right|}{0.4}\right) \tag{6}$$

The next step is to split the above reference wave into many signals of R_y.

$$X = \frac{(N-11)}{4} + 2 \quad Where\ N = 11, 15, 19, 23, \ldots \tag{7}$$

$$R_y = \begin{cases} 1 & \text{if } U_{Low,ref} > y \\ 0 & \text{if } U_{Low,ref} < y \end{cases} \tag{8}$$

Where y = 1 to X. After dividing the reference of the lower inverter into many sub-signals, it is necessary to find out the number of auxiliary switches required for an N level inverter.

$$NAS = \frac{(N-11)}{4} + 12 \quad \text{Where } N = 11, 15, 19, 23, \ldots \tag{9}$$

The main switches of the lower inverter are switched as per the equations given below:

$$MS_5(t) = \left[\overline{R_1} + \overline{R_y}\right] * (Z_1) \tag{10}$$

$$MS_6(t) = \left[R_1 + \overline{Z_1}\right] + \left[\overline{R_1} * Z_1\right] \tag{11}$$

$$MS_7(t) = \left[\overline{R_1} + R_y\right] * Z_1 \tag{12}$$

$$MS_8(t) = \left[R_1 + Z_1\right] + \left[\overline{R_1} * \overline{Z_1}\right] \tag{13}$$

Where y = X, + denotes the logical OR operation and * denotes the multiplication of the signals. The auxiliary switches of the lower inverter can be switched as per the algorithm given below.

1) Step 1: Form a set:

$$R = \left[R_1, R_2, R_3, R_4, \ldots\ldots \quad R_{y-3}, R_{y-2}, R_{y-1}, \quad R_y\right] \tag{14}$$

2) Step 2: Write the permutation P on R as given below:

$$P = \begin{bmatrix} R_1 & R_2 & R_3 & \ldots & R_{y-2} & R_{y-1} & R_y \\ R_2 & R_3 & R_4 & \ldots & R_{y-1} & R_y & R_1 \end{bmatrix} \tag{15}$$

3) Step 3: Remove the last column in the above permutation P1 and rewrite as:

$$P_1 = \begin{bmatrix} R_1 & R_2 & R_3 & \ldots & R_{y-3} & R_{y-2} & R_{y-1} \\ R_2 & R_3 & R_4 & \ldots & R_{y-2} & R_{y-1} & R_1 \end{bmatrix} \tag{16}$$

4) Step 4: From the above equation, it is very easy to derive the switching pulses for all of the auxiliary switches of the N level inverter. The first and last columns of the above matrix are responsible for developing the switching patterns for the first and last auxiliary switches and the equations for AS_1 and AS_n are:

$$AS_1(t) = \left((R_1 \oplus R_2) * \overline{Z_1}\right) + \left((R_{y-1} \oplus R_y) * Z_1\right) \tag{17}$$

$$AS_n(t) = ((R_1 \oplus R_2) * Z_1) + \left((R_{y-1} \oplus R_y) * \overline{Z_1}\right) \quad (18)$$

Where $\oplus$ denotes the XOR operation. Similarly, the 2nd column from the first and 2nd columns from the last of the permutation matrix P_1 are responsible for developing the switching patterns of AS_2 and $AS_{(n-1)}$ and the equations are:

$$AS_2(t) = \left((R_2 \oplus R_3) * \overline{Z_1}\right) + \left((R_{y-2} \oplus R_{y-1}) * Z_1\right) \quad (19)$$

$$AS_{n-1}(t) = ((R_2 \oplus R_3) * Z_1) + \left((R_{y-2} \oplus R_{y-1}) * \overline{Z_1}\right) \quad (20)$$

The above procedure can be repeated to generate the switching patterns for any pair of auxiliary switches based on the following cases.

CASE I (If P_1 contains an odd number of columns): Sometimes as in the case of a 19 level inverter, when X = 4, the number of R signals available will be four (i.e.) R_1; R_2; R_3 and R_4. The number of auxiliary switches in the 19 level inverter will be three. As per the algorithm, the permutation P1 will be:

$$P_1 = \begin{bmatrix} R_1 & R_2 & R_3 \\ R_2 & R_3 & R_4 \end{bmatrix} \quad (21)$$

The first and last columns of the above P1 will be responsible for constructing the switching patterns for AS_1 and AS_3. However, for developing the switching pattern for AS_2, only the center column of the permutation P1 should be used. The switching pattern for AS_2 can be developed as:

$$AS_2(t) = R_2 \oplus R_3 \quad (22)$$

The possibility of CASE I is also valid for N = 11, 19, 27, 35, 43....

CASE II (If P_1 contains an even number of columns): In the case of a 23 level inverter, when X = 5, the number of R signals available will be five (i.e.) R_1, R_2, R_3, R_4 and R_5 whereas the number of auxiliary switches in the 23 Level inverter will be four. As per the algorithm, the permutation P1 will be:

$$P_1 = \begin{bmatrix} R_1 & R_2 & R_3 & R_4 \\ R_2 & R_3 & R_4 & R_5 \end{bmatrix} \quad (23)$$

The first and last columns of the above P_1 will be responsible for constructing the switching patterns for AS_1 and AS_4, and the 2nd and 3rd columns are used for developing the switching pattern for AS_2 and AS_3. Columns 2 and 3 have only three unique R signals (i.e.) R_2, R_3 and R_4 to develop the switching patterns for AS2 and AS3.

$$AS_2(t) = \left((R_2 \oplus R_3) * \overline{Z_1}\right) + \left((R_3 \oplus R_4) * Z_1\right) \quad (24)$$

$$AS_3(t) = ((R_2 \oplus R_3) * Z_1) + \left((R3 \oplus R_4) * \overline{Z_1}\right) \quad (25)$$

The possibility of CASE II is also valid for N = 15, 23,31, 39, 47 etc. The modulation index M_a of the proposed N level inverter is defined as:

$$M_a = \frac{A_{pr}}{M\ A_{pc}} \quad (26)$$

Where $M = \frac{(N-1)}{2}$, N = 11,15,19,23...etc

Where A_{pr} represents the peak value of the modulating or reference wave and A_{pc} represents the peak to peak value of the carrier (triangular) wave. The main switches MS_1 and MS_3 are switched by comparing the reference waveform R_{01} with the carrier wave. As a result, the voltage V_{xz} between points x and z in Fig. 1 appears as shown in Fig. 3. The main switches MS_2 and MS_4 are switched by comparing the reference waveform R_{02} with the carrier wave. As a result, the voltage V_{yz} between points y and z in Fig. 1 appears as shown in Fig. 3. The main switches of the lower bridge inverter MS_5 - MS_8 are switched as per equations (10)-(13) and auxiliary switch AS_1 is switched as per the above proposed algorithm, as shown in Fig. 3. The proposed generalized algorithm is very simple since it makes use of simple logical operations.

IV. Converter Losses

The average switching power loss P_{sloss} in the switch during the transition of switch is given by:

$$P_{sloss} = \frac{1}{2} V_{DC} I_{DC} f_s \left(t_{c(on)} + t_{c(off)}\right) \quad (27)$$

Where $t_{c(on)}$ and $t_{c(off)}$ are the turn on and turn off cross over intervals, respectively; V_{DS} is the voltage across the switch and I_{dc} is the current which flows through the switch. For the sake of clarity, the proposed topology with 15 levels is compared with familiar, similar topologies. For simplification, the proposed topology and the well-known inverter topologies are assumed to operate at the same turn-on and turn-off crossover intervals and at the same I_{dc}. Then, the average switching power loss P_{sloss} is proportional to V_{DS} and f_s.

$$P_{sloss} \propto V_{DC} f_s \quad (28)$$

The number of primary devices required for generating 15 levels in the proposed inverter is 10 and the voltage across these switches is V_{DC} for the upper H-bridge switches (4 numbers), $6V_{DC}$ for the lower H-bridge switches (4 numbers) and $4V_{DC}$ for the auxiliary switches (2 numbers). The upper H-bridge inverter switches at a high frequency f_s, the lower H-bridge inverter switches at the fundamental frequency fm and the auxiliary devices switch twice at the fundamental frequency (2fm). Therefore, the switching losses of the proposed inverter can be written as:

$$\begin{aligned} P_{sloss(proposed)} &= 4V_{DC} f_s + 4(6V_{DC}) f_m + 2(4V_{DC})(2 f_m) \\ &= 4V_{DC}\left[f_s + 6 f_m + 4 f_m\right] \\ &= 4V_{DC}\left[f_s + 10 f_m\right] \end{aligned} \quad (29)$$

Similarly, the number of primary devices required for generating 15 levels in the MLISPC inverter is 14 and the voltage across these switches is V_{DC} for the upper H-bridge switches (4numbers), $6V_{DC}$ for the lower H-bridge switches (4 numbers) and $2V_{DC}$ for the series/parallel switches (6 numbers). The upper H-bridge inverter switches at a high frequency f_s, the lower H-bridge inverter switches at the fundamental frequency fm and the series/parallel switches switch twice at the fundamental frequency ($2f_m$). Therefore, the switching losses of

TABLE III
SIMULATION PARAMETERS

PARAMETERS	LEVEL 11	LEVEL 15	LEVEL 43
Value of M	5	7	21
Upper inverter	65V	47V	15.5V
Lower inverter	130V	94V	31V
Load resistance and inductance: 100Ω &30mH. Filter Inductance and capacitance: 1.5 mH& 12.5μF			

the proposed inverter can be obtained as:

$$P_{sloss(proposed)} = 4V_{DC}f_s + 4(6V_{DC})f_m + 2(6V_{DC})(2f_m) \quad (30)$$
$$= 4V_{DC}[f_s + 6f_m + 6f_m]$$
$$= 4V_{DC}[f_s + 12f_m]$$

Likewise, for conventional symmetrical CHB inverters, the switching losses can be calculated as:

$$P_{sloss(symm,CHB)} = 28V_{DS}f_s \quad (31)$$

For an asymmetrical cascaded H bridge inverter with 1:2:4 configurations, the switching losses can be obtained as:

$$P_{sloss(asymm,CHB)} = 28V_{DS}f_s \quad (32)$$

Since $f_s >> f_m$ and from equations (27)-(32), it is evident that among the various familiar topologies, the proposed topology has the lowest switching losses when compared to the other topologies. In the proposed inverter, at any point in time, the number of switches in conduction is only 4 (2 from the upper inverter and 2 from the lower inverter). Therefore, the conduction losses P_{closs} of the proposed inverter are:

$$P_{csloss} = 4R_{ON}I^2 \quad (33)$$

Where R_{ON} is the internal resistance of the switching device and I is the current flowing into the devices. In the case of the MLISPC topology, the number of conducting devices increases as the number of levels increases. This in turn, increases the conduction losses. The same is true for all of the well-known topologies. Hence, the conduction losses are lower in the case of the proposed topology when compared to the MLISPC, the conventional symmetrical CHB and asymmetrical CHB inverters.

V. SIMULATION RESULTS

To validate the proposed inverter topology, simulations are carried out for the proposed inverter in Matlab/Simulink. The algorithm discussed in Section III is implemented in the simulations up to 43 levels and it can be extended to any required level. The conditions set for simulation and experiment are same. Table III gives the simulation parameters for 11, 15 and 43 level inverters. The upper inverter is operated at a high switching rate that is equivalent to the carrier frequency (i.e. 10 kHz), while the lower inverter is operated at a low frequency (nearly equal to the fundamental frequency i.e. 50Hz). Fig. 6 shows the simulation results for the load voltage of the 11 level inverter together with the upper and lower inverter voltages for a modulation index of M_a= 1. When the modulation index is reduced from 1, the number of voltage levels at the load also decreases. Fig. 7 shows the output across the load and the upper and lower inverters for the modulation index M_a= 0.8 (i.e. when the value of A = 4).

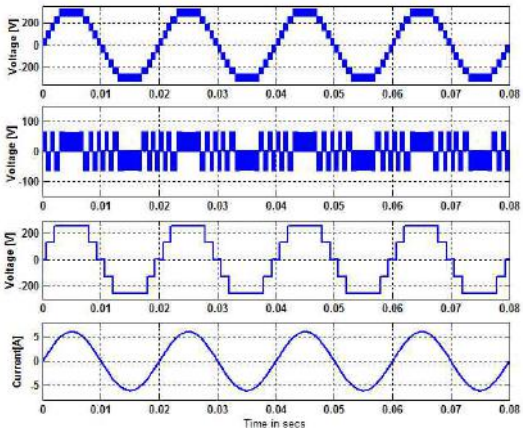


Fig. 6. (a) Voltage across the load (11 Levels). (b) Voltage across the upper inverter $V_{up.}$ (c) Voltage across the lower inverter $V_{low.}$ (d) Load Current waveform for modulation index M_a=1.

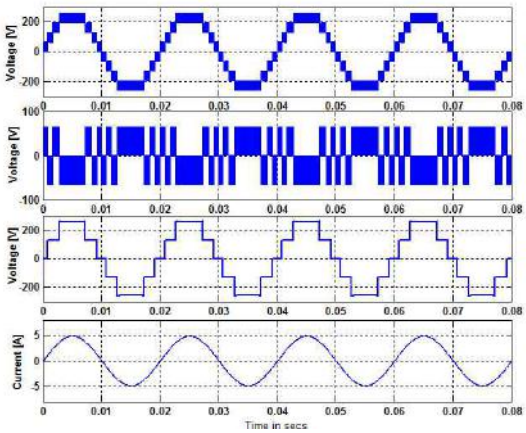


Fig. 7. (a) Voltage across the load (9 Levels). (b) Voltage across the upper inverter $V_{up.}$ (c) Voltage across the lower inverter $V_{low.}$ (d) Load Current waveform for modulation index Ma=0.8.

From Fig. 6 and Fig.7 it is observed that when the modulation index is reduced from 1 to 0.8, the output voltage across the load has only nine levels. Any further reduction in the modulation index will reduce the number of voltage levels at the load end. For example, when M_a = 0.6 i.e. A = 3 the number of levels obtained at the load voltage is seven, when M_a = 0.4 i.e. A = 2 the voltage level at the load becomes five and so on. Fig. 8 shows the resultant waveforms of a 15 level inverter along with the upper and lower inverter waveforms for a modulation index of Ma= 1 (i.e. A = 7). Any further decrease in the value of A leads to a reduction in the output voltage levels. For example, when A =5, it generates an 11 level output as shown in Fig. 6. Fig. 9 shows the simulation results of a 43 level inverter along with the upper and lower inverters, in which the load voltage is very close to sinusoidal. Table IV gives the details of the total harmonic distortion at the load voltage and current for various output voltage levels.

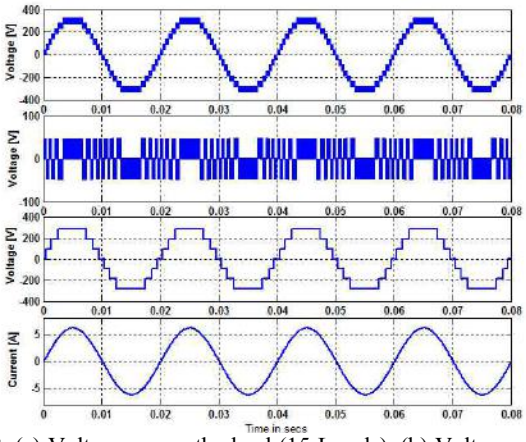


Fig. 8. (a) Voltage across the load (15 Levels). (b) Voltage across the upper inverter $V_{up.}$ (c) Voltage across the lower inverter $V_{low.}$ (d) Load Current waveform for modulation index M_a=1.

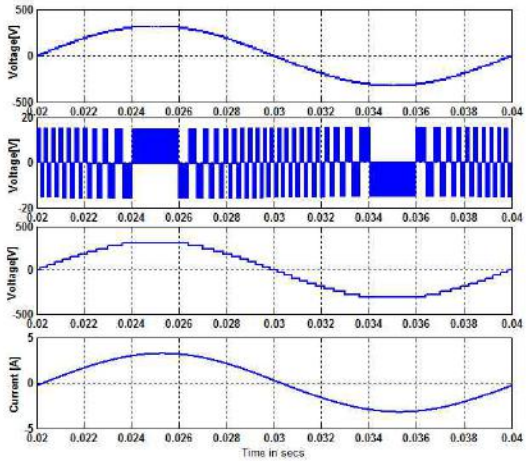


Fig. 9. (a) Voltage across the load (43 Levels A = 21). (b) Voltage across the upper inverter $V_{up.}$ (c) Voltage across the lower inverter $V_{low.}$ (d) Load Current waveform for modulation index M_a=1.

TABLE IV
THD FOR VOLTAGE AND CURRENT FOR VARIOUS LEVELS

		Voltage THD		Current THD	
Levels	A	WOF	WLCF	WOF	WLCF
43	21	2.67	0.03	1.83	0.87
15	7	7.98	0.06	4.98	1.06
13	6	9.21	0.03	6.34	1.82
11	5	11.27	0.09	8.09	2.32
9	4	14.34	0.03	10.57	4.29
7	3	19.48	0.20	14.19	4.89
5	2	28.86	0.05	18.79	5.67
3	1	56.7	0.80	20.28	8.53
WOF-Without Filter			WLCF-With LC Filter		

VI. EXPERIMENTAL RESULTS

Fig. 10 shows a schematic diagram for the hardware setup of the proposed inverter, developed in the laboratory, for 15 levels. The upper and lower inverters consist of MKI 80-06T6K series IGBTs. The auxiliary switch used in the lower inverter is a

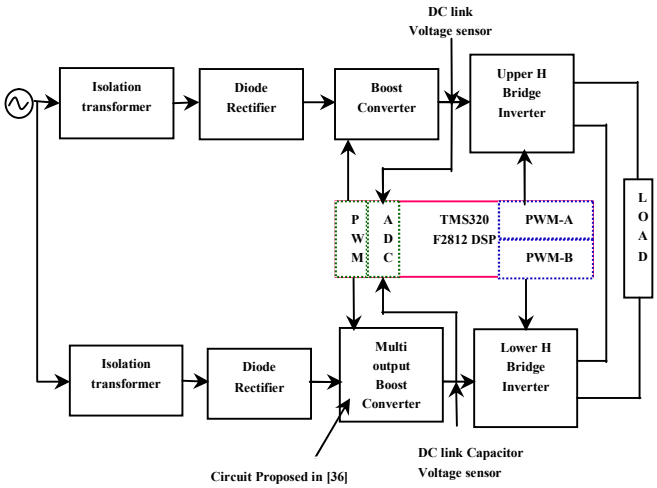


Fig. 10. Schematic diagram for the hardware Setup of the proposed inverter (15 Levels).

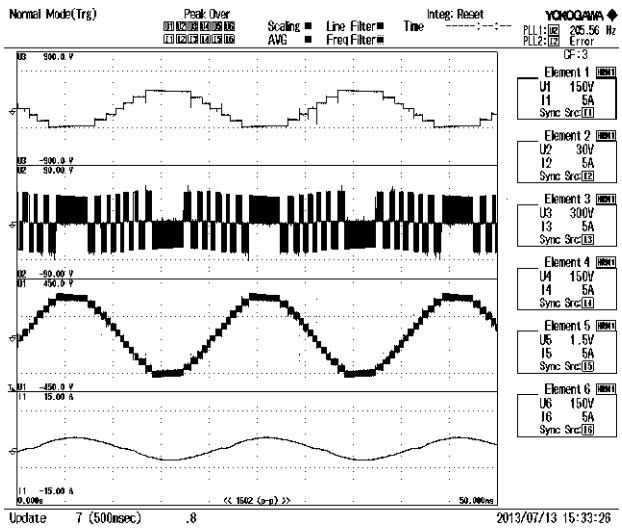


Fig. 11. Hardware results (a)Voltage across the lower inverter V_{low} (b)Voltage across the upper inverter V_{up} (c) Voltage across the load (15 Levels) (d) Load Current waveform for modulation index M_a=1.

FIO50-12BD bidirectional device. The gate driving signal is developed by using a TMS320F2812 Texas instruments DSP. The programs for the TMS320F2812 DSP are composed with code composer studio and Matlab/Simulink. Fig. 11 shows the experimental results of a 15 level inverter with a modulation index of 1 and a switching frequency of 10 KHz. The prototype inverter is made to drive an RL load with the values of R and L indicated in Table III.

Fig. 12 shows the hardware results of a 15 level inverter with and without a filter. The values of the LC filter used in the hardware prototype are similar to those of the simulation environment. A study very similar to the simulation is done in the hardware prototype for various modulation indices. Fig. 13 shows the experimental results of a 15 level inverter when the

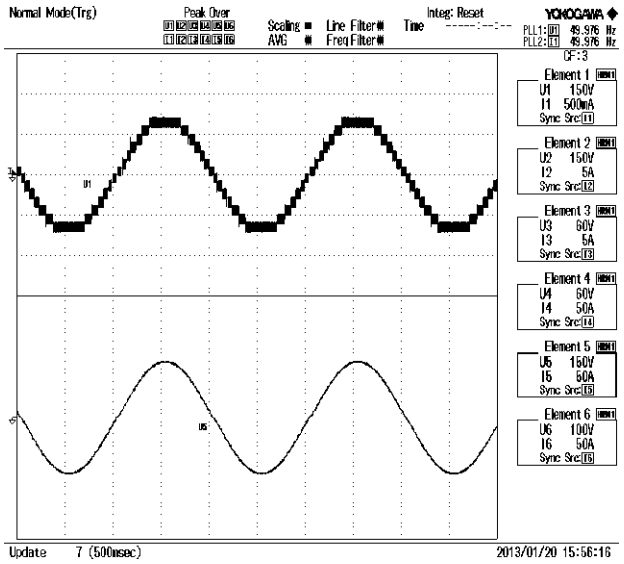


Fig. 12. Hardware results (a) Voltage across the load (15 Levels) with out filter (b) With LC filter.

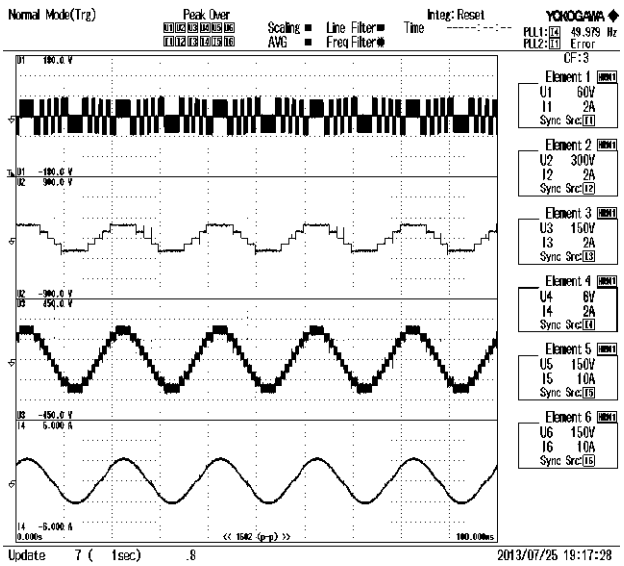


Fig. 13. Hardware results When 15 level inverter is driven by M_a=0.7.(a)Voltage across the upper inverter V_{up} (b) Voltage across the lower inverter V_{low} (c) Voltage across the load (11 Levels) (d) Load Current waveform.

modulation index is reduced to 0.7 (i.e. when A = 5), which leads to an 11 level output at the load terminals.

Fig. 13 includes the waveforms of the upper and lower inverter along with the load current waveform for M_a = 0.7. Fig. 14 shows the hardware results of a 15 level inverter when driven by a modulation index of 0.4, which leads to a 7 level output at the load terminals. Fig. 15 presents the total harmonic distortion content of the voltage, current and power obtained from the hardware prototype along with the load voltage for a 15 level inverter when driven with a modulation index of 0.4, which leads to a 7 level output. As indicated in Table IV, the THD values obtained from the simulation and the results obtained

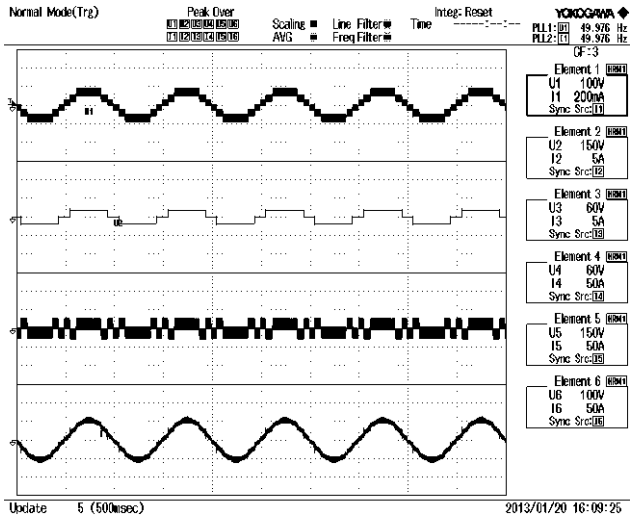


Fig. 14. Hardware results When 15 level inverter is driven by M_a=0.4.(a)Voltage across the load (7 Levels) (b) Voltage across the lower inverter V_{low}(c) Voltage across the upper inverter V_{up} (d) Load Current waveform

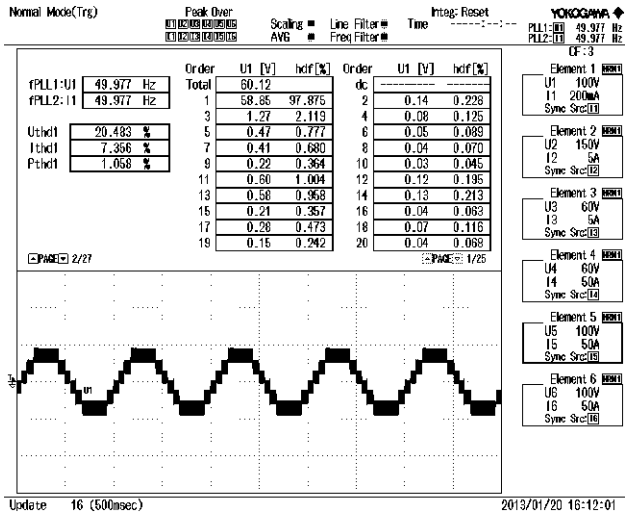


Fig. 15. Harmonic Spectrum of 15 level inverter when drive by M_a=0.4.(a)Numerical Values of Voltage, Current and Power THD (b)Inverter load voltage (7 Level output).

from the hardware prototype match well for a 7 level inverter without a filter. In order to study the performance of the proposed inverter, the inductive load is varied over a wide range. Fig. 16 and Fig. 17 show the load voltage and current waveforms of the proposed inverter for various power factors. It is evident from the load profile waveforms that the proposed inverter is also capable of supplying power to a highly inductive load.

In order to validate the proposed multilevel inverter fed from a multi output DC-DC boost converter, a step change in the reference values of the lower DC link capacitors were given at 0.5 secs (i.e. a change from 50 Volts to 100 Volts). Similarly a step change in the upper boost converter is given at

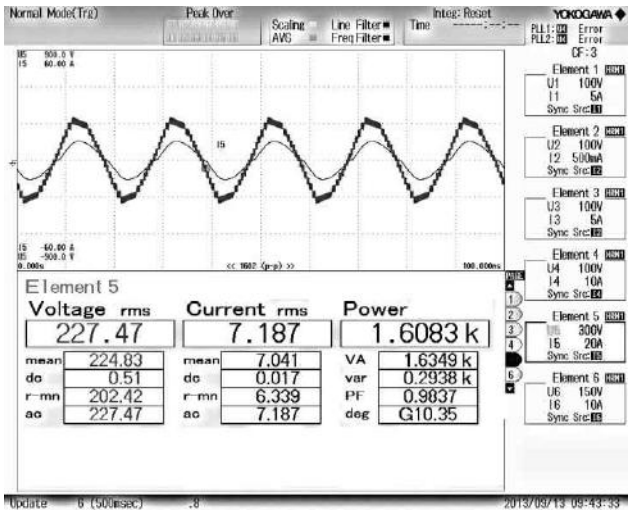


Fig. 16. Load voltage and current waveform for power factor of 0.9837.

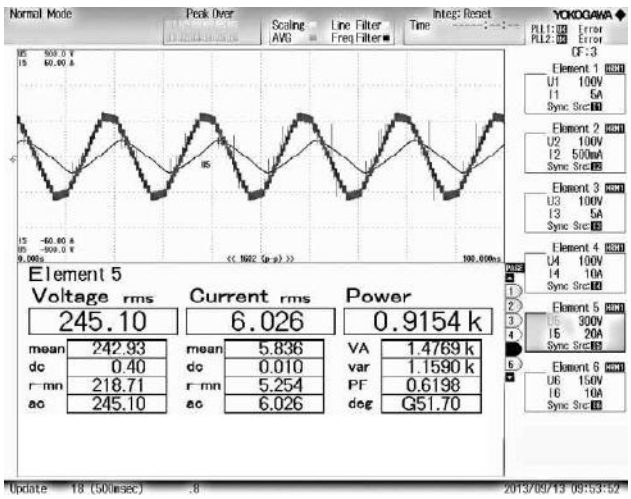


Fig. 17. Load voltage and current waveform for power factor of 0.6198.

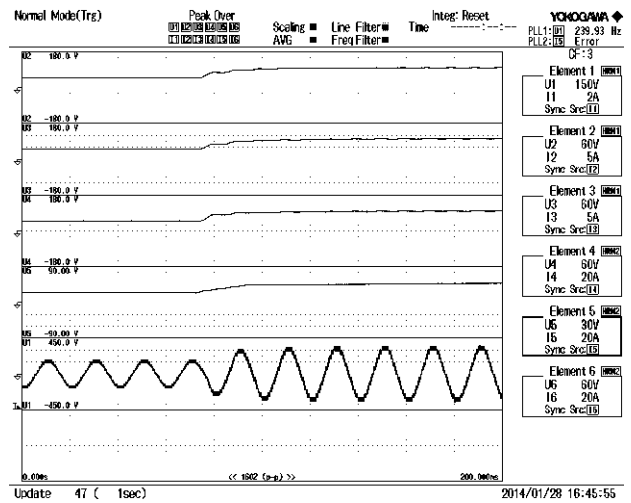


Fig. 18. Step response in Capacitor voltages of lower inverter along with load voltageobtained from the simulation and the results obtained from thehardware prototype match well for a 7 level inverter withoutfilter.

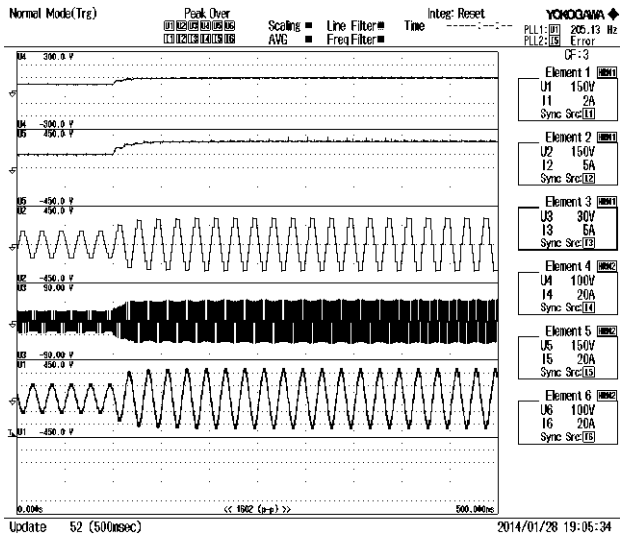


Fig. 19. Step response in capacitor voltages of upper and lower inverter along with upper, lower and load voltage waveform.

0.5 secs (i.e. from 25 Volts to 50 Volts) in order to maintain the ratio between the lower and upper inverter DC link voltages as two. Fig 18 shows the experimental waveforms of the upper and lower capacitor voltages due to a step change in their reference values (i.e. the upper capacitor voltage is changed from 25 Volts to 50 Volts and the lower capacitor voltages are changed from 50Volts to 100 Volts). Fig 19 shows the corresponding changes in the upper inverter and lower inverter voltages along with the load voltage.

VII. CONCLUSIONS

Multilevel inverters offer enhanced output waveforms with a minimum of THD. This paper presents a novel single phase multilevel inverter with reduced switching devices and isolated DC sources. Simulations are carried out in MATLAB/Simulink and the proposed inverter is implemented in real time using a DSP board. A generalized switching algorithm which can be used for any number of levels is also presented. The performance of the suggested novel multilevel inverter is investigated in detail. Modulation waveforms and harmonic analyses are presented for various values of the modulation indices. By properly adjusting the modulation index, the required number of levels for the inverter output voltage can be achieved. The simulation and experimental results match perfectly with each other. The proposed inverter system offers the advantage of a reduced number of switching devices and isolated DC sources when compared to the conventional CHB and MLISCP for the same number of output levels. In addition, the high frequency switching devices are operated at a low voltage and the low frequency devices are operated at a high voltage. Thus, it can be concluded that the proposed novel multilevel inverter can be used for medium and high power applications.

REFERENCES

[1] C. Govindaraju and K. Baskaran, "Efficient hybrid carrier based space vector modulation for a cascaded multilevel inverter," *Journal of Power Electronics*, Vol. 10, No. 3, pp. . 277-284, May 2010.

[2] M. G. H. Aghdam, S. H. Fathi, and G. B. Gharehpetian, "Harmonic optimization techniques in multi-level voltage-source inverter with unequal DC sources," *Journal of Power Electronics*,Vol. 8, No. 2, pp. . 171-180, Apr. 2008.

[3] E. Babaei, A. Dehqan, and M. Sabahi, "Improvement of the performance of the cascaded multilevel inverters using power cells with two series legs," *Journal of Power Electronics*, Vol. 13, No. 2, pp. 223-231, Mar. 2013.

[4] Y. Zhang, G. P. Adam, T. C. Lim, S. J. Finney, and B. W. Williams, "Mathematical analysis and experiment validation of modular multilevel converters," *Journal of Power Electronics*, Vol. 12, No. 1, pp. 33-39, Jan. 2012.

[5] M. K. Menshawi and S. Mekhilef, "Multistage inverters control using surface hysteresis comparators," *Journal of Power Electronics*,Vol. 13, No. 1, pp. 59-69, Jan. 2013.

[6] N.-V. Nguyen, H.-T. Quach, and H.-H. Lee, "Novel single-state PWM technique for common-mode voltage elimination in multilevel inverters," *Journal of Power Electronics*, Vol. 12, No. 4, PP. 548-558, Jul. 2012.

[7] Y.-M. Park, H.-S. Ryu, H.-W. Lee, M.-G. Jung, and S.-H. Lee, "Design of a cascaded h-bridge multilevel inverter based on power electronics building blocks and control for high-performance," *Journal of Power Electronics*, Vol. 10, No. 3, pp. 262-269, May 2010.

[8] H. Kim, "Filter design for grid-connected single-phase inverters," *Journal of Power Electronics*, Vol. 9, No. 4, pp. 623-630, Jul. 2009.

[9] S.-J. Oh and M.-H. Sunwoo, "Variable structure PWM controller for highly efficient PV inverters," *Journal of Power Electronics*, Vol. 9, No. 6, pp. 866- 873, Nov. 2009.

[10] H. Kim and S.-K. Sul, "A novel filter design for output LC filters of PWM inverters," *Journal of Power Electronics*, Vol. 11, No. 1, pp. 74-80, Jan. 2011.

[11] E. Babaei, "Charge balance control methods for a class of fundamental frequency modulated asymmetric cascaded multilevel inverters," *Journal of Power Electronics*, Vol. 11, No. 6, pp. 811-818, Nov. 2011.

[12] E. Besery, B. Arifoglu, S. Camur, and E. K. Beser,"Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source," *Journal of Power Electronics* , Vol. 10, No. 2, pp. 138-145, Mar. 2010.

[13] V. G. Agelidis, D. M. Baker, W. B. Lawrance, and C. V. Nayar, "A multilevel PWM inverter topology for photovoltaic applications," in *Proc. the IEEE International Symposium on Industrial Electronics* (*ISIE'97)*, Vol. 2, No. 6, pp. 589-594, 1997.

[14] G. Ceglia, V. Guzmn, C. Snchez, F. Ibez, J. Walter, and M. I. Gimnez, "A new simplified multilevel inverter topology for DC-AC conversion," *IEEE Trans. Power. Electron.*, Vol. 21, No. 5, pp. 1311-1319, Sep. 2006.

[15] Y. Hinago and H. Koizumi, "A single-phase multilevel inverter using switched series/parallel DC voltage sources," *IEEE Trans. Ind. Electron*.,Vol. 57, No. 8, pp. 2643-2650, Aug. 2010.

[16] N. A. Rahim and J. Selvaraj, "Multi string five-level inverter with novel PWM control scheme for PV application," *IEEE Trans. Ind. Electron*., Vol. 57, No. 6, pp. 2111-2123, Jun. 2010.

[17] S.-J. Park, F.-S.Kang, M. H. Lee, and C.-U.Kim, "A new single-phase five-level PWM inverter employing a deadbeat control scheme," *IEEE Trans. Power Electron.*, Vol. 18, No. 3, pp. 831-843, May 2003.

[18] S. M. Dehghan, M. M. Diany, and A. Yazdian, "Current-type nine-switch inverters," *Journal of Power Electronics*, Vol. 10, No. 2, pp. 146-154, Mar. 2010.

[19] J. Zhang, Y. Zou, M. Zhang, and K. Ding,"Study on a modified cascade inverter with hybrid modulation," *4th IEEE International Conference on Power Electronics and Drive Systems*, Vol. 1 pp. 379-383, Oct. 2001.

[20] J. Dixon and L. Moran, "High-level multi step inverter optimization using a minimum number of power transistors," *IEEE Trans. Power Electron*, Vol. 21, No. 2, pp. 330-337, Mar. 2006.

[21] N. V. Nho, Q. T. Hai, and H.-H. Lee, "Carrier based single-state PWM technique for minimizing vector errors in multilevel inverters," *Journal of Power Electronics*, Vol. 10, No. 4, pp. 357-364, Jul. 2010.

[22] K. K. Gupta S. Jain, "Multilevel inverter topology based on series connected switched sources," *IET Power Electronics*, Vol. 6, No. 1, pp. 164-174, Jan. 2013 .

[23] N. V. Nho and M. J. Youn, "A unified carrier based PWM method in multilevel inverters," *Journal of Power Electronics*, Vol. 5, No. 2, pp. 142-150, Apr. 2005.

[24] N. A. Rahim, K. Chaniago, and J. Selvaraj, "Single-phase seven-level grid-connected inverter for photovoltaic system," *IEEE Trans. Ind. Electron*., Vol. 58, No. 6, pp. 2435-2443, Jun. 2011.

[25] R. Salehi, N. Farokhnia, M. Abedi, and S. H. Fathi, "Elimination of low order harmonics in multilevel inverters using genetic algorithm," *Journal of Power Electronics*, Vol. 11, No. 2, pp. 132-139, Mar. 2011.

[26] S. Du, J. Liu, and J. Lin, "Leg-balancing control of the DC-link voltage for modular multilevel converters," *Journal of Power Electronics*, Vol. 12, No. 5, pp. 739-747,Sep. 2012.

[27] E. Babaei, "Optimal topologies for cascaded sub-multilevel converters," *Journal of Power Electronics*, Vol. 10, No. 3, pp. 251-261, May 2010.

[28] D. Sha, Z. Guo, K. Deng, and X. H. Liao, "Parallel connected high frequency AC Link inverters based on full digital control," *Journal of Power Electronics*, Vol. 12, No. 4, pp. 595- 603, Jul. 2012.

[29] M. F. Kangarlu, E. Babaei, and M. Sabah, "Cascaded cross-switched multilevel inverter in symmetric and asymmetric conditions," *IET Power Electronics*, Vol. 6, No. 6, pp. 1041-1050, Jul. 2013.

[30] Y. Zhang, G. Adam, S. Finney, and B. Williams, "Improved pulse-width modulation and capacitor voltage-balancing strategy for a scalable hybrid cascaded multilevel converter," *IET Power Electronics*, Vol. 6, No. 4, pp. 783-797, Apr. 2013.

[31] K. Ding, K. W. E. Cheng, and Y. P. Zou, "Analysis of an asymmetric modulation method for cascaded multilevel inverters," *IET Power Electronics*, Vol. 5, No. 1, pp. 74-85, Jan. 2012 .

[32] S. De, D. Banerjee, K. Siva kumar, K. Gopakumar, R. Ramchand, and C. Patel, "Multilevel inverters for low-power application," *IET Power Electronics*, Vol. 4, No. 4, pp. 384-392, Apr. 2011.

[33] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters – State of the art, challenges, and requirements in industrial applications," *IEEE Trans. Ind. Electron*., Vol. 57, No. 8, pp. 2581-2596, Aug. 2010.

[34] A. Dey, P. P. Rajeevan, R. Ramchand, K. Mathew, and K.

Gopakumar, "A space-vector-based hysteresis current controller for a general n-level inverter-fed drive with nearly constant switching frequency control," *IEEE Trans. Ind. Electron*., Vol. 60, No. 5, pp. 1989- 1998, May 2013.

[35] N. A. Rahim, M. F. M. Elias, and W. P. Hew, "Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," *IEEE Trans. Ind.Electron*., Vol. 60, No. 8, pp. 2943- 2956, Aug. 2013.

[36] A. A. Boora, A. Nami, F. Zare, A. Ghosh, and F. Blaabjerg, "Voltage sharing converter to supply single phase asymmetrical four level diode clamped inverter with high power factor loads," *IEEE Trans. Power Electron.,* Vol. 25, No. 10, pp. 2507-2520, Oct. 2010.

Kaliamoorthy Mylsamy received his B E in Electrical and Electronics Engineering at Madras University, Chennai, India, in 1999, and his M.Tech degree in Electrical Drives and Control from Pondicherry University, Puducherry, India, in 2006. He was a gold medalist for the academic years 2004-2006. He has one decade of teaching experience for under graduate and post graduate students of electrical and electronics engineering. He is presently working as an Associate Professor in the Department of Electrical and Electronics Engineering, PSNA College of Engineering and Technology, Dindigul, Tamil Nadu, India. His current research interests include alternative energy sources, fuel cells, energy conversion, multilevel inverters, analysis and control of power electronics devices, power quality and active harmonic analysis. For further details please visit www.kaliasgoldmedal.yolasite.com

Rajasekaran Vairamani was born in Madurai, Tamil Nadu, India, in 1971. He received his B.E degree in Electrical and Electronics Engineering, ME . degree in Power Systems, and his Ph.D. degree from Madurai Kamaraj University, Madurai, Tamil Nadu, India, in 1994, 1997 and 2007, respectively. He is presently heading the Electrical and Electronics Department, PSNA College of Engineering and Technology, Dindigul, Tamil Nadu, India. He is a certified Energy Auditor. His current research interests include power systems, energy, power quality and power electronics energy.

Gerald Christopher Raj Irudayaraj was born on January 7, 1977. He received his B.E., in Electrical and Electronics Engineering from Madurai Kamaraj University, Madurai, Tamil Nadu, India, in 1999, and his M.E. and Ph.D. degrees in Power Electronics and Drives from Anna University, Chennai, Tamil Nadu, India, in 2006 and 2013, respectively. He is presently working as an Associate Professor in the Department of Electrical and Electronics Engineering, PSNA College of Engineering and Technology, Dindigul, Tamil Nadu, India. His current research interests include power electronics and drives, current source inverters, AC drives and applications.

Hubert Tony Raj Lawrence received his B.E degree in Electrical and Electronics Engineering from the FX Engineering College, Thirunelveli, Tamil Nadu, India, in 2011, and his M.E degree in Power Electronics and Drives from the PSNA College of Engineering and Technology, Dindigul, Tamil Nadu, India, in 2013. At present he is working as Assistant Professor in the Department of Electrical and Electronics Engineering, Christian College of Engineering and Technology, Ottanchatram, Tamil Nadu, India. His current research interests include multilevel inverters and induction motor drives. He has a particular interest in the study of power electronics for real time applications.