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Single phase nine level inverter using single DC source supported by capacitor voltage balancing algorithm

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Abstract: This study introduces a new single phase nine-level inverter using two capacitors and a single DC source. Voltage imbalances in the capacitors are eliminated using two control algorithms namely charging algorithm and discharging algorithm. The charging algorithm is used to change the inverter switching states when the measured voltage across the capacitors is less than the prescribed value. Alternatively, if the voltage across the capacitors is greater than the set value, the discharging algorithm determines the switching pattern of the inverter switches. The proposed voltage balancing algorithm is very simple to implement and makes the proposed inverter attractive for industrial applications. An extensive comparison of the proposed inverter is made against other topologies proposed in the literature in terms of the components used. The proposed inverter is tested in both standalone and grid connected modes. The proposed inverter is simulated and implemented as a prototype in the laboratory. Experimental results obtained from the prototype confirm the high-quality transient performance of the proposed inverter in terms of its dc capacitor voltage balancing capability.

1 Introduction

In recent days, IEEE 519-1992 and IEEE 519-2014 standards have made the researchers to investigate more on synthesising staircase voltage waveform using multilevel inverters (MLIs) for high-power applications [1, 2]. However, the MLIs are also used in low- and medium-power applications, especially in transferring power efficiently from renewable energy (RE) sources (like fuel cells, photovoltaic systems etc.) to the load [3, 4]. An MLI is generally a connecting configuration of several input DC levels (acquired either from many isolated DC sources or splitting a single DC source into many voltage levels by using capacitors) and power electronic switches to produce a staircase voltage waveform. Furthermore, power devices used in the MLI experience lesser voltage stress, when compared to the peak level of the load voltage [5, 6]. The MLIs offer many advantages such as enhanced quality of load voltage, i.e. lower total harmonic distortion (THD) when compared with conventional two-level inverters, compact output filters, lessen dv/dt stress and lower electromagnetic interference [7, 8].

The harmonic content in the multilevel waveform can be brought down by increasing the number of levels. On the contrary, this leads to a rise in a number of independent DC sources, power devices, and its associated gate driver circuits. These demands use of hefty transformers, diode bridges and a complicated control strategy to switch the devices, thereby reducing the reliability and efficiency of the system. Hence, restricting the number of power electronic devices and DC sources in power converter topologies is an aggressive field of investigation among the researchers, which leads to producing more voltage levels with minimum devices and isolated DC sources [9–11]. In this connection, researchers have added many MLI topologies to the literature with a minimum number of power electronic devices, but with two or more isolated DC sources [12–14]. On the other hand, if the number of isolated DC source is restricted to one, either the number of power electronic devices increases [15, 16] or the power devices in the topology demands high frequency of operation, many sensing elements, and large DC link capacitors to regulate voltage [17, 18].

This proposed topology is an improved version of the topology proposed in [19–21]. The topology presented in [19] has two isolated DC sources and six power semiconductor devices. Furthermore, the topology presented in [19] can be operated in symmetrical mode (i.e. the voltage magnitude of two isolated DC sources being equal) and asymmetrical mode (i.e. the voltage magnitude of two isolated DC sources being 1:3) to generate five and seven voltage levels at the output side. The topology of [19] is suitable for grid connected RE applications, but with a compromise on a number of devices, sensing elements and demands a complex control strategy to control maximum power point tracking (MPPT), DC link voltage and grid voltage as presented in [22]. The topology discussed in [20] is also a good candidature for grid connected RE applications, which is capable of generating seven levels with one isolated DC source and three DC capacitors with complex voltage regulating algorithm. To increase the number of levels by two more (i.e. nine), the topology in [20] requires one more device and an additional DC bus. The topology offered in [21] is also the best option for grid connected RE applications, but it generates only seven levels with six switches. To increase the levels further by two, it requires two more additional devices and one isolated DC source or a capacitor with the complex control strategy. Increasing the number of isolated DC sources, increases the sensing devices to perform MPPT in RE applications, which increases the size and the cost? On the other hand, if the isolated DC source is replaced with a capacitor, which demands a complex control strategy, the voltage across it has to be regulated.

This study introduces a new structure of MLI capable of generating nine levels with only one DC source and seven power electronic devices (six unidirectional and one bidirectional device). The bidirectional device used in this topology has one insulated-gate bipolar transistor (IGBT) surrounded by four diodes packed in a single chip (FIO 50-12BD).

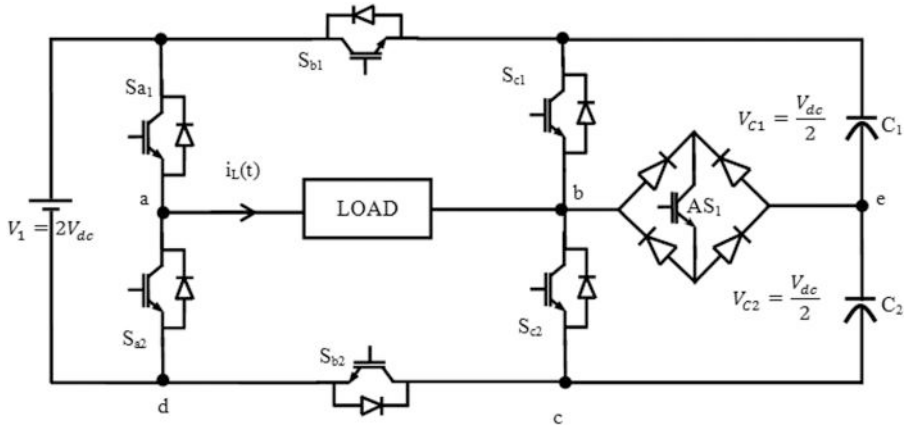

Fig. 1 *Proposed nine-level inverter topology*

The main advantage of this device over other bidirectional devices is that it requires only one gate driver circuitry, whereas a common collector and common emitter configuration based bidirectional devices requires two drivers. Furthermore, the physical dimension of the single chip packed bidirectional device is almost similar to that of the unidirectional device of the same ratings. Hence a single chip packed bidirectional device does not occupy any extra space during implementation, which reduces the size of the inverter.

The proposed topology has two capacitors whose voltage is balanced by using combined switching of two algorithms, namely charging and discharging algorithms. The charging algorithm charges both the capacitors whereas discharging algorithm discharges both the capacitors. The proposed voltage balancing algorithm is tested in both high-power and low-power applications. The proposed topology can be used as an interface between RE sources and the grid.

2 Proposed topology

The proposed single phase nine-level inverter topology is shown in Fig. 1. It consists of seven power devices and two DC capacitors. The various modes of operation of the proposed inverter are explained with the help of equivalent circuits as shown in Fig. 2. The switching states of the proposed inverter are given in Table 1.

It is necessary to indicate that the switches S_{b1} and S_{b2} are complementary to the switches S_{a1} and S_{a2} in all the switching states, where as switches $S_{c}1$ and S_{c2} are complementary to each other in most of the states, except in states S_2, S_5, S_8 and S_{11}. In states S_2, S_5, S_8 and S_{11} both S_{c1} and S_{c2} are in OFF condition. A notable constraint in the switching logic is if A_{S1} is ON switches S_{c1} and S_{c2} are in OFF state, else switches S_{c1} and S_{c2} are in the complementary state. It is clear from Table 1, by maintaining the capacitor voltages V_{C1} and V_{C2} at one-fourth of the input supply voltage (i.e. $V_{C1} = V_{C2} = V_{dc}/2$) is possible to get nine levels at the load. All possible nine levels are shown in the last column of Table 1.

The entire Table 1 can be subdivided into three modes, i.e. charging mode, discharging mode and no effect modes. By clearly investigating on the charging and discharging sub tables of Table 1, switching states S_4 and S_{10} in charging mode (shaded rows of Table 1(a)) are redundant switching states when the capacitor voltage is maintained at half of the DC input voltage (V_{dc}). Similarly switching states S_3 and S_9 of discharging mode (shaded rows of Table 1(b)) are redundant switching states when the capacitor voltage is maintained at half of the DC input voltage (V_{dc}). Table 1(c) shows modes of operation in the inverter where there is no variation in the capacitor voltages. This makes the proposed topology to have flexible voltage across the capacitors. As indicated in Table 1, if the capacitor voltages are maintained at half of the DC input voltage, the proposed inverter is capable of generating nine levels at its load terminals. The capacitor voltage and the DC input voltage are measured and are compared. If the capacitor voltage (sum of V_{C1} and V_{C2}) is less than half of the DC input voltage, then the charging mode of operation is performed as indicated in Table 2(a). On the other hand, if the capacitor voltage (sum of V_{C1} and V_{C2}) is more than that of the DC input voltage the discharging mode of operation is performed as indicated in Table 2(b).

3 Dynamic model

The dynamic model of the proposed nine-level inverter has been derived as follows [23]. Let S_{ai}, S_{bi}, S_{ci} ($i = 1, 2$) and AS_1 be the switching functions of the switches S_{ai}, S_{bi}, S_{ci} and AS_1 switches, respectively. The switching functions are defined as follows:

$$S_{ai} = \begin{cases} 1, & \text{if } S_{ai} \text{ is ON,} \\ 0 & \text{if } S_{ai} \text{ is OFF,} \end{cases} \quad \text{where } i = 1, 2 \tag{1}$$

$$S_{bi} = \begin{cases} 1, & \text{if } S_{bi} \text{ is ON,} \\ 0 & \text{if } S_{bi} \text{ is OFF,} \end{cases} \quad \text{where } i = 1, 2, \tag{2}$$

$$S_{ci} = \begin{cases} 1, & \text{if } S_{ci} \text{ is ON,} \\ 0 & \text{if } S_{ci} \text{ is OFF,} \end{cases} \quad \text{where } i = 1, 2, \tag{3}$$

$$AS_1 = \begin{cases} 1, & \text{if } AS_1 \text{ is ON,} \\ 0 & \text{if } AS_1 \text{ is OFF.} \end{cases} \tag{4}$$

The output voltage of the inverter can be written as

$$V_{ab} = V_{ad} + V_{dc} + V_{ce} + V_{eb}, \tag{5}$$

where the points a, b, c, d, and e are marked in Fig. 1 and each of them can be determined based on the values of the switching functions

$$\begin{cases} V_{ad} = (1 - S_{a2})V_1, \\ V_{dc} = (S_{b2} - 1)[V_1 - (V_{C1} + V_{C2})], \\ V_{ce} = -V_{C2}, \\ V_{eb} = (1 - AS_1)[S_{c2}V_{C2} - S_{c1}V_{C1}]. \end{cases} \tag{6}$$

Substituting (6) into (5)

$$\begin{aligned} V_{ab} &= (1 - S_{a2})V_1 + (S_{b2} - 1)[V_1 - (V_{C1} + V_{C2})] \\ &\quad - V_{C2} + (1 - AS_1)[S_{c2}V_{C2} - S_{c1}V_{C1}] \\ &= (S_{b2} - S_{a2})V_1 - (S_{b2} + S_{c1} - AS_1S_{c1} - 1) \\ &\quad \times V_{C1} - (S_{b2} - S_{c2} + AS_1S_{c2})V_{C2}. \end{aligned} \tag{7}$$

As indicated in Table 1, if AS_1 is ON both S_{c1} and S_{c2} are OFF, hence if (3) and (4) are substituted in (7) AS_1S_{c1} and AS_1S_{c2} in (7) will always be zero. So rewriting (7)

$$V_{ab} = (S_{b2} - S_{a2})V_1 - (S_{b2} + S_{c1} - 1)V_{C1} - (S_{b2} - S_{c2})V_{C2}\,. \quad (8)$$

Equation (8) implies that the switching state of auxiliary switch AS_1 does not play any role in determining the load voltage V_{ab}. Table 3

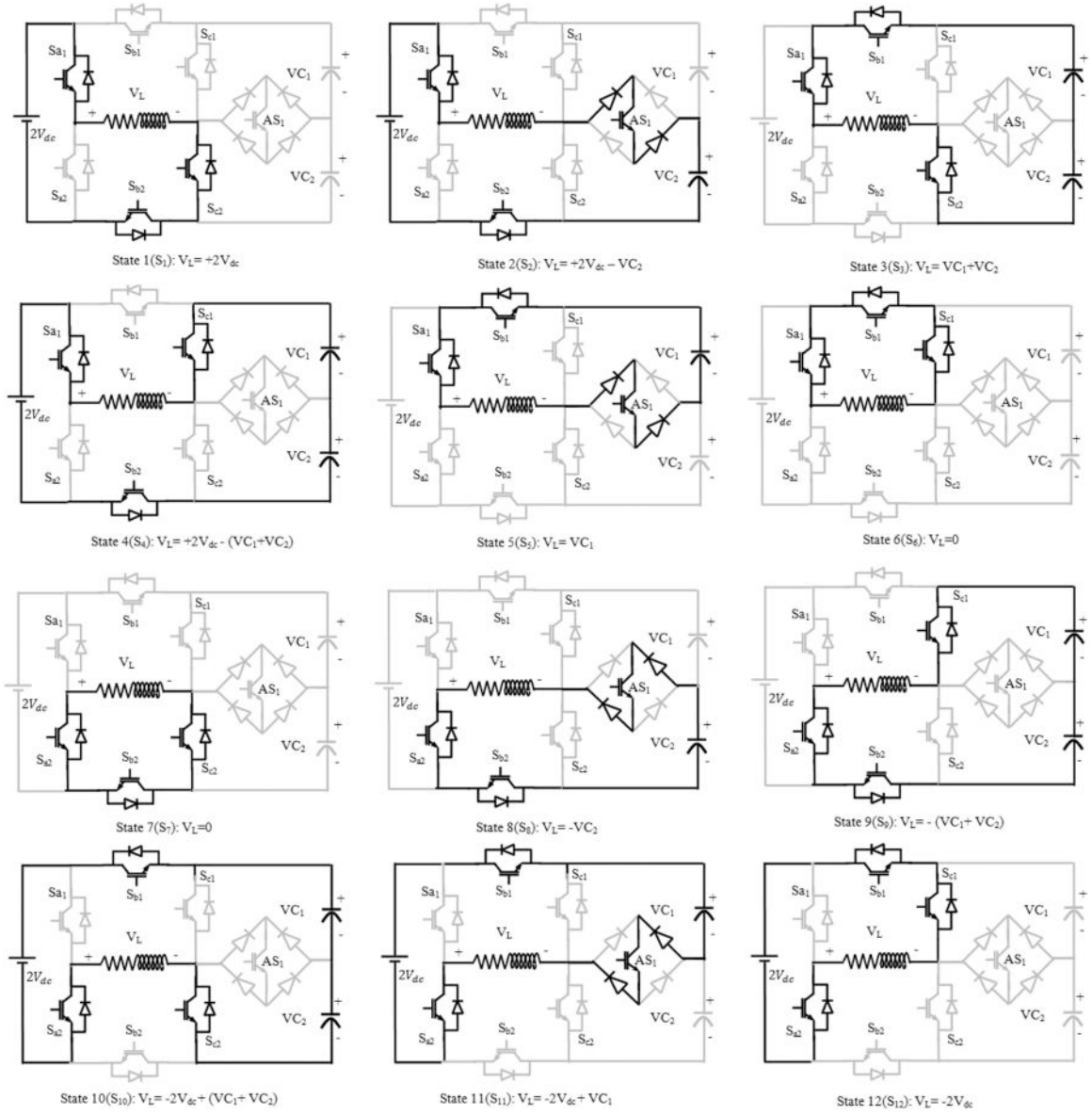

Fig. 2 *Switching states and conducting paths of the proposed inverter*

Table 1 Switching states of the proposed inverter including charging, discharging and no effect modes

State	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c1}	AS_1	Charging		Node voltages		$V_{\text{load}} = V_a - V_b$	$V_{ab} = V_a - V_b$
								C_1	C_2	V_a	V_b		$V_{C1} = V_{C2} = V_{dc}/2$
S_1	on	off	off	on	off	on	off	no effect	no effect	$+2V_{dc}$	0	$+2V_{dc}$	$+2V_{dc}$
S_2	on	off	off	on	off	off	on	no effect	charges	$+2V_{dc}$	V_{C2}	$+2V_{dc} - V_{C2}$	$\frac{+3V_{dc}}{2}$
S_3	on	off	on	off	off	on	off	discharges	discharges	V_{C1}	$-V_{C1}$	$V_{C1} + V_{C2}$	$+V_{dc}$
S_4	on	off	off	off	on	off	off	charges	charges	$+2V_{dc}$	$V_{C1} + V_{C2}$	$+2V_{dc} - (V_{C1} + V_{C2})$	$+V_{dc}$
S_5	on	off	on	off	off	off	on	discharges	no effect	V_{C1}	0	V_{C1}	$\frac{+V_{dc}}{2}$
S_6	on	off	on	off	on	off	off	no effect	no effect	0	0	0	0
S_7	off	on	off	on	off	on	off	no effect	no effect	0	0	0	0
S_8	off	on	off	on	off	off	on	no effect	discharges	$-V_{C2}$	0	$-V_{C2}$	$\frac{-V_{dc}}{2}$
S_9	off	on	off	on	on	off	off	discharges	discharges	$-(V_{C1} + V_{C2})$	0	$-(V_{C1} + V_{C2})$	$-V_{dc}$
S_{10}	off	on	on	off	off	on	off	charges	charges	$-2V_{dc}$	$-(V_{C1} + V_{C2})$	$-2V_{dc} + (V_{C1} + V_{C2})$	$-V_{dc}$
S_{11}	off	on	on	off	off	off	on	charges	no effect	$-2V_{dc}$	$-V_{C1}$	$-2V_{dc} + V_{C1}$	$\frac{-3V_{dc}}{2}$
S_{12}	off	on	on	off	on	off	off	no effect	no effect	$-2V_{dc}$	0	$-2V_{dc}$	$-2V_{dc}$

State	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	AS_1
Charging Mode							
S_2	ON	OFF	OFF	ON	OFF	OFF	ON
S_4	ON	OFF	OFF	ON	ON	OFF	OFF
S_{10}	OFF	ON	ON	OFF	OFF	ON	OFF
S_{11}	OFF	ON	ON	OFF	OFF	OFF	ON
Discharging Mode							
S_2	ON	OFF	ON	OFF	OFF	ON	OFF
S_4	ON	OFF	ON	OFF	OFF	OFF	ON
S_{10}	OFF	ON	OFF	ON	OFF	OFF	ON
S_{11}	OFF	ON	OFF	ON	ON	OFF	OFF
Noeffect Mode							
S_1	ON	OFF	OFF	ON	OFF	ON	OFF
S_6	ON	OFF	ON	OFF	ON	OFF	OFF
S_7	OFF	ON	OFF	ON	OFF	ON	OFF
S_{12}	OFF	ON	ON	OFF	ON	OFF	OFF

Table 2 Charging and discharging of capacitors for one cycle

State	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	AS_1	State	S_{a1}	S_{a2}	S_{b1}	S_{b2}	S_{c1}	S_{c2}	AS_1
S_1	on	off	off	on	off	on	off	S_1	on	off	off	on	off	on	off
S_2	on	off	off	on	off	off	on	S_2	on	off	off	on	off	off	on
S_4	on	off	off	on	on	off	off	S_3	on	off	on	off	off	on	off
S_5	on	off	on	off	off	off	on	S_5	on	off	on	off	off	off	on
S_6	on	off	on	off	on	off	off	S_6	on	off	on	off	on	off	off
S_7	off	on	off	on	off	on	off	S_7	off	on	off	on	off	on	off
S_8	off	on	off	on	off	off	on	S_8	off	on	off	on	off	off	on
S_{10}	off	on	on	off	off	on	off	S_9	off	on	off	on	on	off	off
S_{11}	off	on	on	off	off	off	on	S_{11}	off	on	on	off	off	off	on
S_{12}	off	on	on	off	on	off	off	S_{12}	off	on	on	off	on	off	off

(a) charging of capacitors when $V_{C1}, V_{C2} \leq \frac{V_{dc}}{2}$

(b) discharging of capacitors when $V_{C1}, V_{C2} \geq \frac{V_{dc}}{2}$

Table 3 Switching states and load voltage levels

Switching state	S_{a2}	S_{b2}	S_{c1}	S_{c2}	V_{ab}
S_1	0	1	0	1	V_1
S_2	0	1	0	0	$V_1 - V_{C2}$
S_3	0	0	0	1	$V_{C1} + V_{C2}$
S_4	0	1	1	0	$V_1 - (V_{C1} + V_{C2})$
S_5	0	0	0	0	V_{C1}
S_6	0	0	1	0	0
S_7	1	1	0	1	0
S_8	1	1	0	0	V_{C2}
S_9	1	1	1	0	$-(V_{C1} + V_{C2})$
S_{10}	1	0	0	1	$-V_1 + (V_{C1} + V_{C2})$
S_{11}	1	0	0	0	$-V_1 + V_{C1}$
S_{12}	1	0	1	0	$-V_1$

here $V_1 = 2V_{dc}$ and $V_{C1} = V_{C2} = \frac{V_{dc}}{2}$

shows the switching states and load voltage levels calculated from (8).

4 Switching strategy

MLIs are generally switched by using high-switching frequency [24], low-switching frequency [25] or by hybrid switching (combination of high frequency and low frequency) [26]. The high-frequency switching strategy includes the multicarrier pulse-width modulation (PWM) switching strategy [27], multi reference PWM switching strategy [28] and space vector PWM technique [29]. The low-frequency modulation strategy includes selective harmonic elimination [30], active harmonic elimination [31] and fundamental frequency modulation techniques [32].

Any of the above-mentioned switching strategies can be adopted for the proposed topology. In this work, the multi-carrier pulse-width modulation (MCPWM) strategy is used. In the MCPWM strategy, level shifted carrier signals are compared with a single reference signal and the switching pulses obtained from the comparator are given to appropriate switching devices to generate corresponding voltage levels.

In this work, eight carrier signals ($C_1, C_2, \ldots, C_8$) of different amplitudes (level shifted) are compared with a common reference

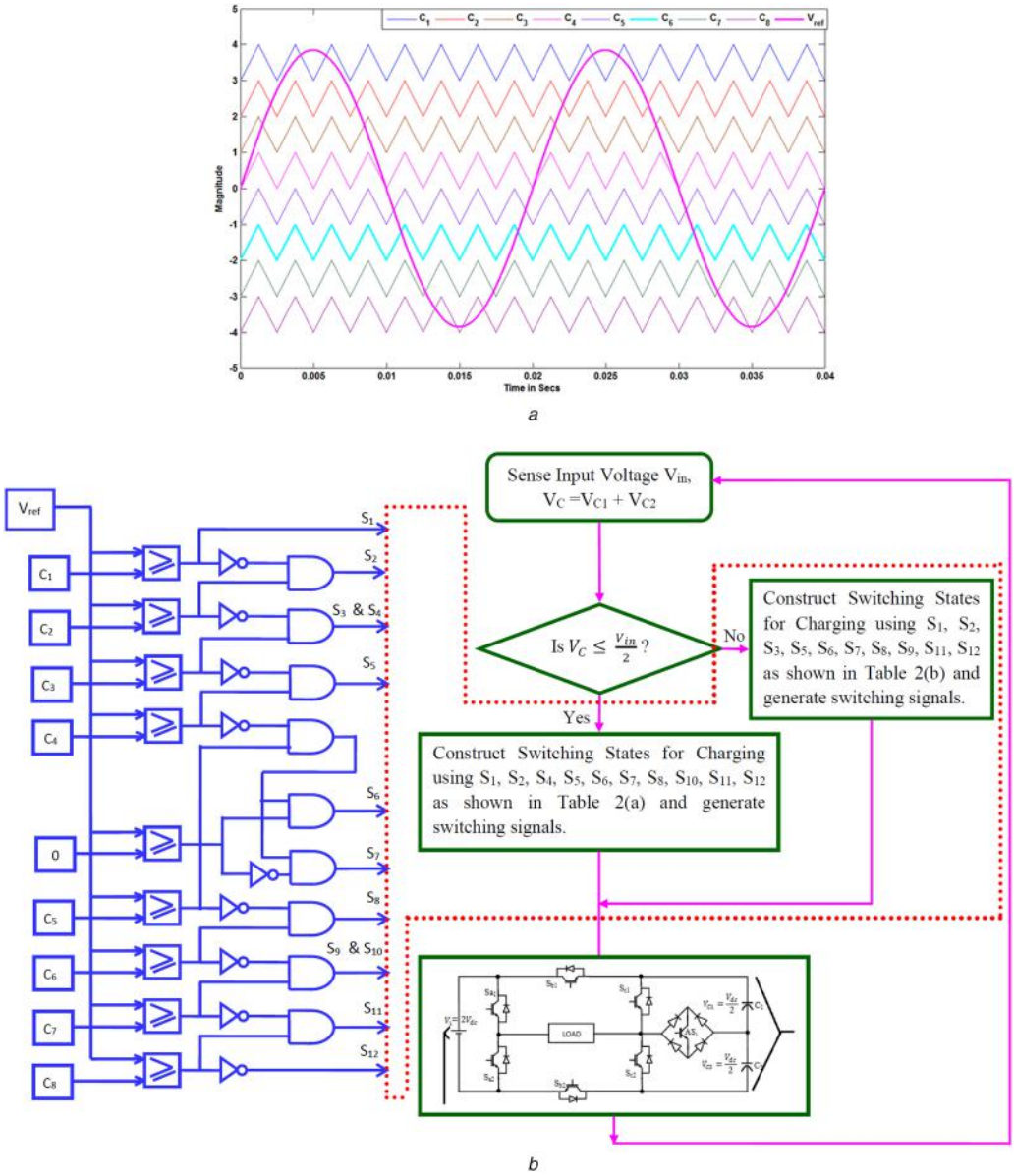

Fig. 3 *Flowchart of capacitor voltage balancing algorithm*
(a) MCPWM Technique with eight carrier signals and the reference signal,
(b) Switching signal generation and capacitor voltage balancing algorithm

as shown in Fig. 3*a* (level shifted carrier and reference signals). The switching pulses corresponding to switching states S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8, S_9, S_{10}, S_{11} and S_{12} (as indicated in Table 3) are generated by comparing a reference signal (V_{ref}) with those carrier signals. It should be noted that the switching states S_3 and S_4 are redundant states when the capacitor voltage is maintained at half of the input DC voltage, i.e. V_{in}. Similarly switching states S_9 and S_{10} were also redundant during the negative half cycle for the same conditions of capacitor voltages. Furthermore, switching states S_6 and S_7 are used to reduce the switching frequency because of their redundant nature.

During the positive half cycle of V_{ref}, switching state S_6 contributes to produce zero level at the output, whereas during the negative half cycle of V_{ref}, switching state S_7 contributes to produce zero level at the output. The control algorithm for the proposed inverter is shown in Fig. 3*b* which can produce a nine-level voltage waveform at the load terminal with fixing the sum of capacitor voltages at half of the input voltage. The input voltage and the total capacitor voltage (i.e. $V_{C1} + V_{C2}$) are sensed and compared. If the sensed capacitor voltage is lesser than half of the input DC voltage (V_{in}) then Table 2(a) switching states are used to increase the capacitor voltage to a value equal to $V_{in}/2$, else if the capacitor voltage is > $V_{in}/2$ then Table 2(b) switching states are used to reduce the capacitor voltage to a value =$V_{in}/2$.

5 Comparative studies with other topologies

This section compares the proposed inverter with other conventional and similar topologies available in the literature. The comparison is made in terms of a number of components used to generate nine levels and voltage blocking capability of the switches.

5.1 Comparison based on the number of components

The proposed topology is compared with other similar topologies with respect to the number of components for producing single phase nine-level output voltage waveform and is consolidated in Table 4.

It is evident that the projected inverter with the voltage-balancing algorithm has fewer components and its implementation complexity of the control algorithm is very less when compared to the other topologies listed in Table 4.

It is necessary to point out that no consistent control techniques have been reported for a neutral point clamped inverter (more than three levels) because they have certain limitations on the

Table 4 Component comparison of proposed topology with other topologies for generating nine levels at the load

Type of inverter	Isolated DC sources	Flying capacitors	Clamping diodes	Number of drivers	Sensors	Total component count	Complexity in control
cascaded H bridge	4	0	0	16	0	20	low
neutral point clamped	8	0	14	16	0	38	very high
flying capacitor	1	7	0	16	0	24	high
Gupta *et al.* [19]	4	0	0	10	0	14	high
Rahim *et al.* [20]	1	4	0	7	4	16	very high
Ounejjar *et al.* [21]	1	2	0	8	4	15	very high
Liu *et al.* [33]	1	2	2	9	0	14	high
Mokhberdoran *et al.* [34]	4	0	0	12	0	16	high
Oskuee *et al.* [35]	4	0	0	10	0	14	high
Hsieh Cheng-Han *et al.* [36]	1	3	4	8	0	16	very high
proposed topology	1	2	0	7	2	12	very low

modulation index and load power factor [27]. It can be observed from Table 4 that the packed U cell inverter developed in [21] matches closely with the proposed inverter in terms of the number of components used to construct the inverter (i.e. only one active switch is lesser in the proposed inverter). Even though Packed U-cell topology is extendable theoretically, they are realised and reported experimentally only up to seven levels [21, 22, 37].

Similarly Packed U-cell topology proposed in [21] has presented simulation and experimental results only for the seven-level output that too with a complex voltage-balancing algorithm as indicated in [22]. Furthermore, the controller design needs an accurate system model which increases the number of state variables and therefore, increases the current and voltage sensors [22]. If Packed U cell topology [21] is extended to nine levels it requires an additional capacitor. Hence, two capacitors are required to generate nine levels in addition to the input DC voltage. Furthermore, the voltages of these capacitors need to be maintained at $V_{dc}/7$ and $3V_{dc}/7$, which requires an extremely complex voltage balancing algorithm which is not reported in [21]. Moreover, this topology requires three sensors (two for voltage and one for current) to implement the voltage balancing algorithm for generating seven levels. If the same topology is extended for nine levels it requires an additional voltage sensor for sensing the voltage of the additional capacitor, which increases the cost. Hence, to control the inverter proposed in [21] to generate nine levels, the controller complexity increases but the control complexity is very less in the case of the proposed inverter.

5.2 Comparison based on voltage-withstanding capability

The proposed inverter is compared with the other analogous topologies based on the voltage withstanding or blocking capability (V_B) of the switches and is presented in Table 5. The comparison is made on the assumption that all the topologies listed in Table 5 are excited with a DC input voltage equal to V_{dc}. From Table 5, the proposed topology has only two switches and has voltage blocking capability as V_{dc}, remaining five switches are rated less than V_{dc}, whereas in other topologies presented in Table 5 the number of switches with V_{dc} voltage blocking capability is higher than the proposed inverter. Hence, only a few switches have higher voltage-blocking capability, which reduces the cost of the power devices.

6 Power loss calculations

The power converter losses are mainly due to the power semiconductor devices. Losses of power semiconductor devices are classified into three categories viz. conduction (or) on state losses (P_C), switching state losses (P_S) and blocking (or) off state losses (P_B). P_C occurs during the on-state of the device, P_S occurs during the switching whereas P_B occurs when the device is in OFF state. During the blocking state of the power semiconductor device, the current flowing through the device is negligible and hence, blocking state losses are negligible. Hence, conduction and switching losses are considered and are presented for the proposed inverter.

6.1 Conduction losses

Conduction losses in the proposed converter are the sum of ON state losses of the IGBT and anti-parallel diode is [26]

$$P_{C,IGBT}(t) = [V_{IGBT} + R_{IGBT}\, i^{\beta}]i(t), \tag{9}$$

$$P_{C,Diode}(t) = [V_{Diode} + R_{Diode}\, i(t)]i(t), \tag{10}$$

where $P_{C,IGBT}(t)$ and $P_{C,Diode}(t)$ denote the instantaneous ON state losses of the IGBT and its anti-parallel diode, respectively. V_{IGBT} and V_{Diode} correspond to the ON state voltage drops of the IGBT and its anti-parallel diode, whereas R_{IGBT} and R_{Diode} indicate their corresponding ON state resistance. The symbol β is a constant governed by the IGBT characteristics. At any instant of time, the conducting IGBT has to carry the load current $i_L(t)$. Furthermore, based on the direction of load current ($i_L(t)$) and the load voltage level, either the IGBT or its anti- parallel diode conducts. For instance, referring to Fig. 2, state 3 (S_3), when the load current $i_L(t) > 0$, then the IGBT S_{a1} and S_{C2} conducts whereas, the anti-parallel diode of the IGBT S_{b1} conducts. Alternatively, during the same state S_3 if the load current $i_L(t) < 0$, then S_{b1} conducts whereas, the anti-parallel diodes of the IGBTs S_{a1} and S_{C2} conducts. Hence, during any instant of time, if $N_{IGBT}(t)$ and $N_{Diode}(t)$ represent the number of IGBTs and diodes conducting, the average conduction losses can be derived by using (9) and (10) and is expressed as

$$\begin{aligned} P_{C,avg} = \frac{1}{\pi}\int_0^{\pi} [\{&N_{IGBT}(t)V_{IGBT} \\ &+N_{Diode}(t)V_{Diode}\}i_L(t) \\ &\{N_{IGBT}(t)R_{IGBT}i_L^{\beta+1}(t) \\ &+N_{Diode}(t)R_{Diode}i_L^2(t)\}]\mathrm{d}(\omega t)\,. \end{aligned} \tag{11}$$

6.2 Switching losses

The switching losses (P_S) are incurred during the instants when the devices change their state, i.e. from OFF state to ON state ($P_{S,ON}$) also termed as turn on losses and from ON state to OFF state ($P_{S,OFF}$) also termed as turn OFF losses. $P_{S,ON}$ and $P_{S,OFF}$ are given by [34]

$$\begin{aligned} P_{S,ON} &= \int_0^{t_{on}} v(t)i(t)\,\mathrm{d}t \\ &= \int_0^{t_{on}} \left[\left\{V_B\frac{t}{t_{on}}\right\}\left\{-\frac{I}{t_{on}}(t-t_{on})\right\}\right]\mathrm{d}t = \frac{1}{6}V_B I t_{on}, \end{aligned} \tag{12}$$

Table 5 Voltage stress comparison proposed topology with other similar topologies

Type of inverter	Active switches		DC capacitors		Clamping diodes	
Number	Voltage blocking capability (V_B)	Number	Voltage blocking capability (V_B)	Number	Voltage blocking capability (V_B)	
cascaded H bridge inverter	16	V_{dc}	0	—	0	—
neutral point clamped	16	$0.25V_{dc}$	4	$0.25V_{dc}$	12	4 diodes: 0.25 V_{dc} 4 diodes: 0.5 V_{dc} 4 diodes: 0.75 V_{dc}
flying capacitor inverter	16	$0.25V_{dc}$	16	V_{dc}	0	—
[19]	10	four switches: V_{dc} six switches: V_{dc}	0	—	0	—
[20]	8	two switches: V_{dc} four switches: $0.5V_{dc}$ two switches: $0.25V_{dc}$	2	0.5 V_{dc}	0	—
[21]	7	four switches: V_{dc} three switches: $0.75V_{dc}$	4	$0.25V_{dc}$	0	—
[33]	9	four switches: $0.25V_{dc}$ two switches: V_{dc} three switches: $0.5V_{dc}$	2	0.5 V_{dc}	2	2 V_{dc}
[34]	12	four switches: V_{dc} eight switches: $2V_{dc}$	0	—	0	—
[35]	10	two switches: $4V_{dc}$ two switches: $3V_{dc}$ two switches: $2V_{dc}$ four switches: V_{dc}	0	—	0	—
[36]	8	V_{dc}	3	$0.33V_{dc}$	4	$0.667V_{dc}$
proposed topology	7	two switches: V_{dc} four switches: $0.5V_{dc}$ one switch: $0.25V_{dc}$	2	$0.5V_{dc}$	0	—

$$P_{S,} = \int_0^{t_{off}} v(t)i(t)\,dt = \int_0^{t_{off}} \left[\left\{V_B \frac{t}{t_{off}}\right\}\left\{-\frac{I}{t_{off}}(t - t_{off})\right\}\right] dt = \frac{1}{6}V_B I t_{off}. \quad (13)$$

The total switching losses are given by

$$P_{S,\,total} = P_{S,ON} + P_{S,} = \frac{1}{6}V_B I(t_{on} + t_{off}). \quad (14)$$

Here V_B indicates the blocking voltage of the switch, t_{on} and t_{off} refers to ON time and OFF time of the switches and I is the current through the switch.

Since there are seven active switches and two diodes conduct at any point in time in the proposed topology, the total switching losses of it can be rewritten as

$$P_{S,total} = \sum_{i=0}^{9} \frac{1}{6}V_{B,i} I(t_{on} + t_{off}) f_i, \quad (15)$$

where $V_{B,i}$ and f_i indicates the blocking voltage and switching frequency of the ith switch, respectively.

7 Simulation and experimental results

To examine the performance of the proposed inverter and its control strategy, a simulation model of the proposed inverter is modelled in MATLAB/SIMULINK tool. Input DC voltage (V_{in}) of 400 V is used. The switching signals obtained are shown in Fig. 4*a*. It shows that the switches S_{a1} and S_{a2} operate at the fundamental frequency of the reference wave, whereas switches S_{b1}, S_{b2}, S_{c1}, S_{c2} and AS_1 switch at the frequency of the carrier wave. Furthermore, the advantage of the proposed inverter configuration is low frequency (i.e. reference frequency) operated switches S_{a1} and S_{a2} are rated to the value of input DC voltage, whereas the high-frequency operated switches (i.e. carrier frequency) S_{b1}, S_{b2}, S_{c1} and S_{c2} are rated at half of the DC input voltage and auxiliary switch operating at carrier frequency is rated at one-fourth of the DC input voltage. Thus, the high-voltage rated switches operate at the fundamental frequency and the low-voltage rated switches operate at high frequency, which reduces the switching losses of the proposed inverter.

The load voltage waveform with nine levels and its harmonic spectrum is shown in Fig. 4*b* for an input dc voltage of 400 V and switching frequency of 5 kHz. The load voltage has a symmetrical voltage step of 100 V ($= V_{C1} = V_{C2}$) and its THD is 15.33%, which is obtained without using any hefty voltage filter at the output. A load current waveform and its harmonic spectrum are shown in Fig. 4*c* for a load of 5 kW@0.8 lagging power factor.

The current THD is just 0.79%. The dynamics of the inverter is tested through simulation by applying step variations at the input voltage and the load. The load voltage dynamics for the sudden change in the input voltage is shown in Fig. 5*a*. At the start-up of the simulation, the input voltage is set to 400 V DC, after few seconds the input voltage is decreased suddenly to 300 V DC again after few seconds it is increased to 400 V DC. During this period the load is also varied from 5 to 2 kW, which reduces the load current as shown in Fig. 5*b*.

The capacitor voltages (both V_{C1} and V_{C2}) are also captured during this dynamic study and are reported in Fig. 5*c*. Initially, both the capacitor voltages are at 100 V for an input DC voltage of 400 V and 5 kW load. After few cycles of this operation when the

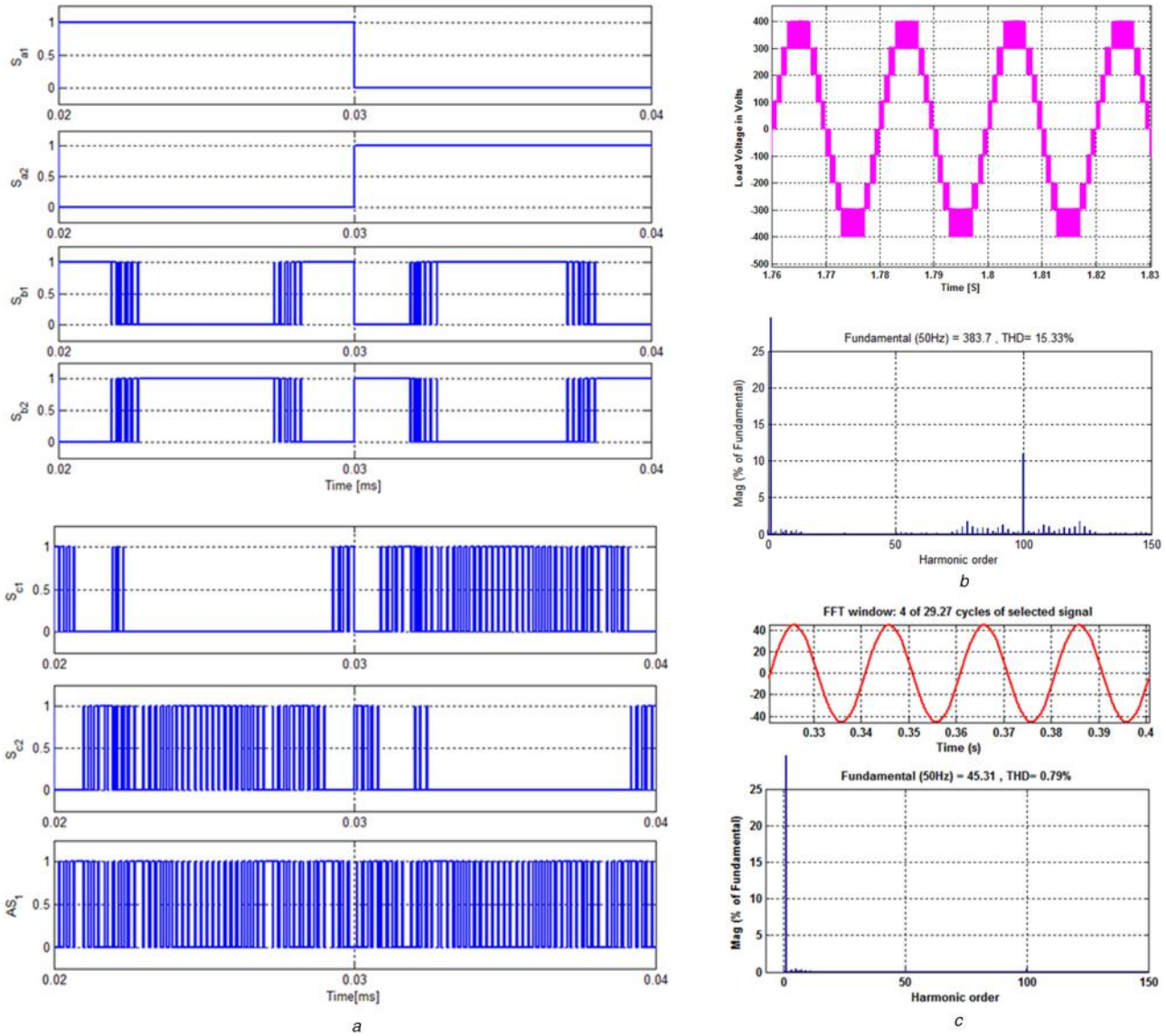

Fig. 4 *Switching signals and harmonic profile (voltage and current)*
(a) Switching pulses of inverter switches,
(b) Load voltage with nine levels and its harmonic spectrum,
(c) Load current waveform and its harmonic spectrum

input DC voltage is reduced to 300 V DC, both the capacitor voltages reduce to 75 V. Following this operation, the input DC voltage is again raised to 400 V DC which increases the capacitor voltages to 100 V. Subsequently, this operation inverter load is decreased from 5 to 2 kW, which reduces the capacitor ripples as shown in Fig. 5*c*.

To validate the proposed nine-level inverter topology, an archetype is built and tested in the laboratory. The control algorithm for the proposed inverter is programmed in a SPATRAN 6 digital signal processing (DSP) board using a XILINX system generator tool box of MATLAB/SIMULINK. The parameters of the prototype developed in the laboratory are listed in Table 6.

The voltage and current waveforms of the laboratory prototype are tested using a key sight DSO-X 3034A oscilloscope. The Amp Flex flexible current is used to sample the inverter currents. Chroma programmable DC power source 62000H series is used as an input source to the inverter. The load voltage waveform of the prototype inverter is shown in Fig. 6. Evidently, the inverter load voltage has nine levels (i.e. ±300, ±225, ±150, ±75 , 0 V).

The modulation index (M_a) of the inverter varied from 1 to 0.6 and the result of the load voltage is presented in Fig. 7. Obviously, due to the variations in M_a, the load voltage levels are also decreased from nine to seven when M_a is reduced from 1 to 0.8. Furthermore, reducing the value of M_a from 0.8 to 0.6 load voltage levels still reduce from seven to five as indicated in the zoomed Fig. 7.

To validate the performance of the proposed capacitor voltage-balancing algorithm, initially, the DC input voltage is set to 300 V in the Chroma programmable DC power source with $M_a = 1$. It is observed from Fig. 8*a* that the load voltage is of nine levels with its peak at 300 V DC and the capacitor voltages are at 75 V. Further to study the transient performance of the voltage balancing algorithm, the input DC voltage of the test bed inverter is reduced from 300 to 180 V. Due to this variation, the total capacitor voltage ($V_{C1} + V_{C2}$) is also reduced from 150 to 90 V. In turn, the individual capacitor voltages are also decreased from 75 to 45 V as shown in Fig. 8*b*. It is worth noting that the capacitor voltage balancing algorithm is realised by changing the input DC source voltage.

Fig. 8*c* shows the load voltage and load current waveform of the proposed inverter. The inverter is loaded till 10 A peak value and the results are presented.

8 Conclusions

A new single phase nine-level inverter using two capacitors and a single DC source is proposed. The great benefit of the proposed inverter is to attain the nine-level output voltage with just seven power electronic devices. Various states of operation of the proposed inverter are detailed with mathematical equations related

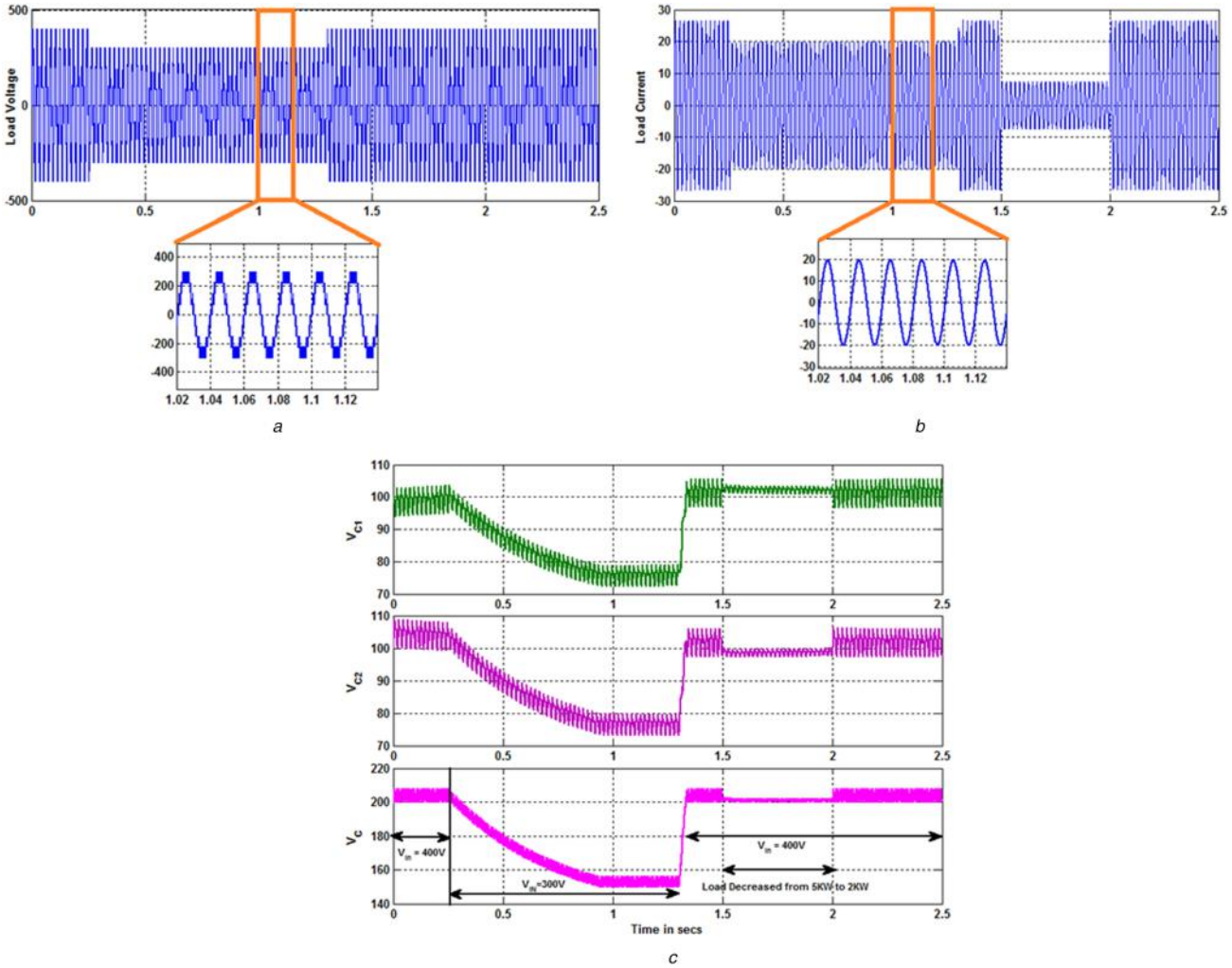

Fig. 5 *Dynamic performance*
(a) Dynamic load voltage variations for dynamic changes in input voltage,
(b) Dynamic load current variations for dynamic changes in input voltage and load,
(c) Capacitor voltage (V_{C1}, V_{C1} and $V_{C1} + V_{C2}$) for dynamic variations in Input voltage and load

Table 6 Simulation and experimental parameters

Parameter	Value
source voltage (DC)	300 V
DC capacitor	4700 F
switching frequency	5 kHz
switches	
S_{a1}-S_{a2}, S_{b1}-S_{b2}, S_{c1}-S_{c2},	FGL40N120AND
switch AS1	FIO 50-12BD
buffer IC	IC 74HC244P
driver IC	HCPL3120
controller	Spatran 6A DSP
solver (simulation)	ode15s (stiff/NDF)
RL load	50 Ω, 25 mH

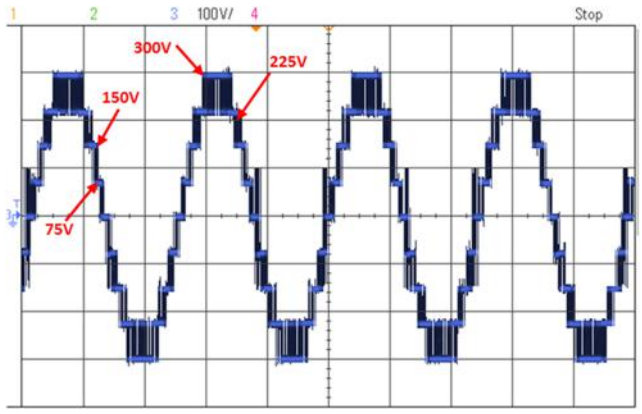

Fig. 6 *Experimental Load Voltage*

to load voltage, conduction losses, switching losses and voltage stress of the switches. A capacitor voltage-balancing algorithm is also proposed for the developed inverter, which maintains the capacitor voltage even for sudden variations in the DC input voltage. The proposed inverter is simulated and its results are validated in the prototype developed in the laboratory. The proposed inverter is compared with the conventional MLIs and other superior inverter proposed in the literature. The comparison result unveils that the proposed inverter reduces the switching devices and the other associated auxiliary circuits when compared with the other similar topologies. The proposed inverter is the best candidature for medium- and high-power applications.

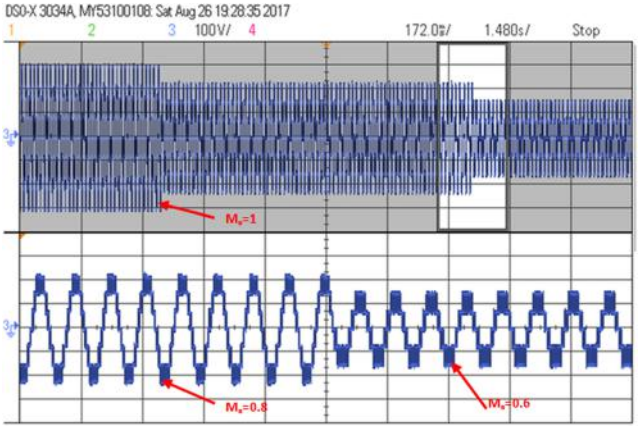

Fig. 7 *Load voltage waveform for different values of modulation index*

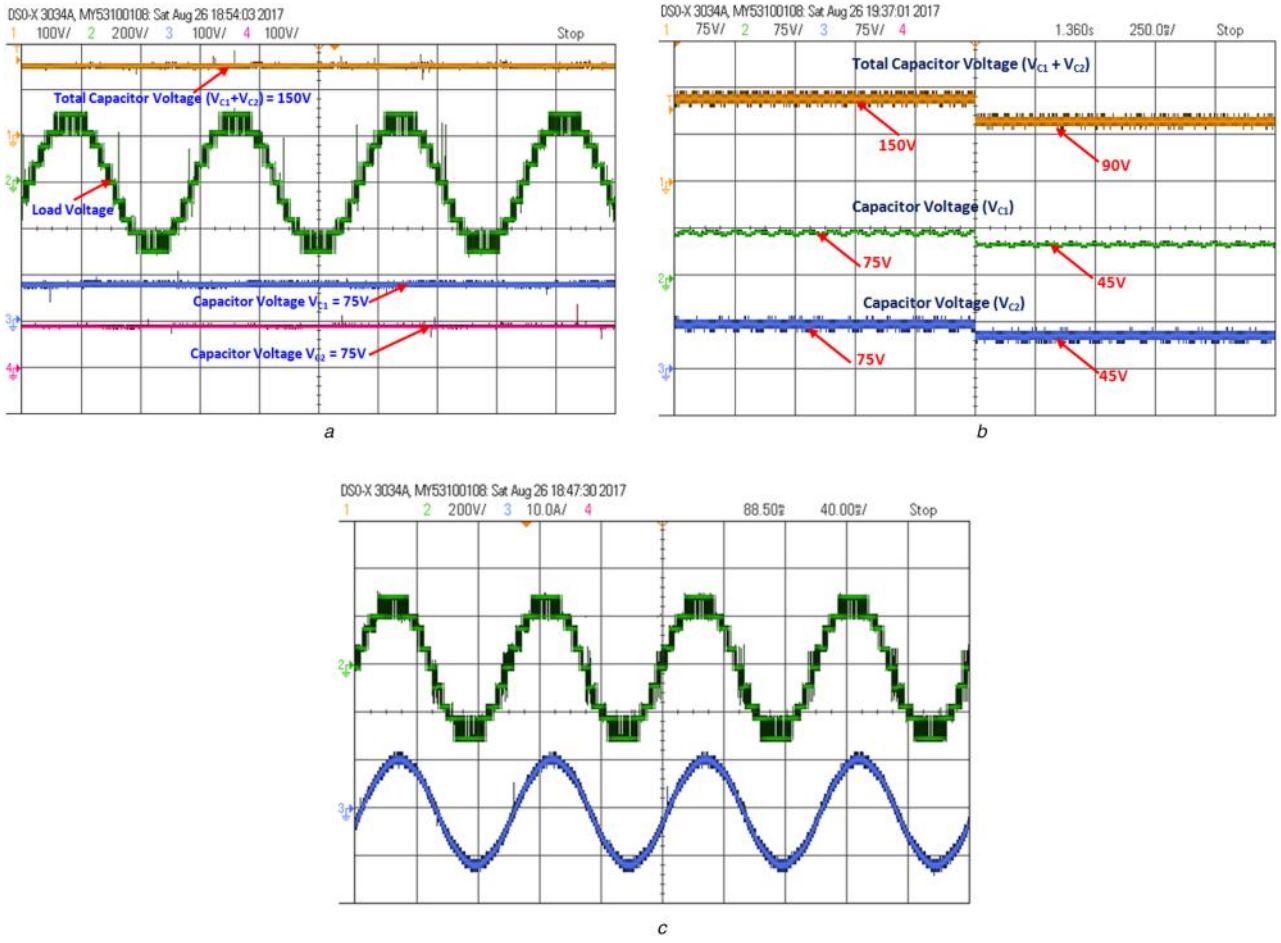

Fig. 8 *Experimental Waveforms*

(a) Load voltage and capacitor voltages for DC input voltage of 300 V,

(b) Capacitor voltages for the sudden change in DC input voltage from 300 to 180 V,

(c) Load voltages and load current waveform of the proposed inverter

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