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A Modified Asymmetrical Single-Phase Multilevel Inverter Topology for Enhanced Power Quality

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Abstract: This paper proposes a modified Asymmetrical Single-Phase Multilevel Inverter (ASP-MLI) with minimum number of power semiconductor devices. This inverter is extendable to any number of levels by cascading the basic units. The basic unit consists of two isolated DC sources and six power electronic devices, out of which two devices are bidirectional. This modified inverter is driven by three switching schemes. Among the three schemes, the last scheme is capable of generating more number of levels when compared to the remaining two schemes for the given number of power electronic devices and isolated DC sources. The modified ASP-MLI is compared with the conventional asymmetrical multilevel inverter in terms of number of power devices and Total Harmonic Distortion (THD). The proposed ASP-MLI is simulated using MATLAB/SIMULINK and the results are presented.

Key words: Asymmetrical Multilevel Inverter · Switching schemes · Total Harmonic Distortion · Power semiconductor devices · Output levels

INTRODUCTION

The ever increasing energy demand, exhausting nature of fossil fuels and their growing prices and environmental problems caused by CO_2 emissions from conventional power plants have attracted researchers to concentrate on renewable energy based power generation systems. Among the various sources of renewable energies, wind and photovoltaic are the most promising and are very popular. Energy generated from wind and photovoltaic can be fed into the grid through inverters. Such inverters are called as grid connected inverters.

A single-phase grid connected inverters are mostly used in low-power or residential applications, whose power demand is less than 10kW [1]. Various types of single-phase inverters investigated in the literature are detailed in [2]. A common used topology in grid connected applications is full bridge inverter with three level output voltage. In order to satisfy the IEEE 519 harmonic standards, the three level inverter is to be operated at high frequency [3]. But this eventually increases the switching losses, acoustic noise and Electro Magnetic Interference (EMI) problems to other equipments [4]. Quality of output voltage can be improved by reducing the harmonic content in it, which in turn reduces the size of the filter and the level of EMI generated by the inverter during its switching operation [5, 6].

Quality of output voltage of an inverter can be improved by using multilevel inverters [MLI]. MLIs have nearly sinusoidal output voltage and current waveforms with improved harmonic profile, less stress in power electronic switches due to reduced voltages, lower switching losses when compared to conventional three level inverters, smaller filter size and reduced EMI [7].

In recent years various MLIs are proposed in the literature. Among those commonly used types are diode-clamped MLI, capacitor clamped MLI, cascaded H-bridge MLI and modified H-bridge MLI [8-11]. Cascaded H-bridge and Modified H bridge inverters are further classified into symmetrical and asymmetrical MLIs. Asymmetrical MLIs (ASMLI) are capable of producing

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more levels for the given power electronic devices when compared with Symmetrical MLIs (SMLI) [12]. This paper proposes a novel single phase asymmetrical MLI with minimum number of power semiconductor devices. The validity of the proposed inverter is verified through simulation using MATLAB/SIMULINK.

Section II describes about the circuit topology of the proposed ASP-MLI. In Section III various-proposed schemes of ASP-MLI are compared with conventional asymmetrical multilevel inverter. Section IV presents the conclusion of the scheme.

Section II Asymmetrical Single-Phase Multilevel Inverter Topology: The proposed topology consists of a two bidirectional switches added to the conventional H-bridge inverter. The proposed topology has been derived from the topology proposed in [13]. The topology proposed in [13] has only one bidirectional switch which is capable of generating only five levels and is of symmetrical type. Whereas the topology proposed in [13] has two bidirectional switches which is capable of generating seven levels, but it has the problem of capacitor voltage balancing when fed to high power loads [12].

Further the MLI proposed in [14] is again of symmetrical in nature. The asymmetrical MLI proposed in this paper requires only two bidirectional switches to generate seven levels further the problem of capacitor voltage balancing does not exist. Fig. 1 shows basic block of the proposed ASP-MLI topology.

Fig. 2 shows the modes of operation of the proposed ASP-MLI. In Fig. 2 the conducting paths are shown in dark black lines whereas the non-conducting paths are shown in the light grey colors. Table 1 shows the switching table of the basic block of the proposed ASP-MLI, which is capable of generating seven levels.

Further the proposed ASP-MLI is capable of generating higher levels if the basic blocks are connected in cascade.

Fig. 3 shows the cascaded connection of two basic blocks of the proposed ASP-MLI. Any how the number of basic blocks connected in cascade can be increased to increase the number of levels. The cascaded configuration shown in Fig. 3 is capable of generating higher levels which is dependent on the magnitude of the DC voltages. Three different methods are proposed in this paper to select the magnitude of the DC voltage. These methods are analyzed one by one as follows.

Proposed Scheme:1 (Multiples of Five Method): In this scheme the DC voltage is chosen as multiples of five i.e. if the voltage sources in the first basic block are taken as V_{DC} then the voltage sources in the second basic block are chosen as $5V_{DC}$ and that of the third basic block voltages are $25V_{DC}$ and so on. The detailed switching logic for two basic blocks with $V_{DC1} = V_{DC2} = 1V_{dc}$ and $V_{DC3}=V_{DC4} = 5V_{dc}$ is given in Table 2. The maximum possible number of levels in this method is given by

$$Number\ of\ Levels = 5^N \quad (1)$$

Here N is the number of basic blocks of the proposed inverter. Simulation of the proposed cascaded ASMLI driven by this method is simulated using MATLAB/SIMULINK and the results of load voltage and current are shown in Fig. 4.

Proposed Scheme:2 (Multiples of Two Method): Like the conventional cascaded H bridge inverter, the voltage sources amplitude is chosen in binary geometric proposition i.e. 1:2:4 ratios. Here again the same circuit topology shown in Fig. 3 is considered with voltage magnitudes of DC sources as given below,

$V_{DC1} = V_{dc}$, $V_{DC2} = 2V_{dc}$,

$V_{DC3} = 4V_{dc}$, $V_{DC4}= 8V_{dc}$

The detailed switching table of the proposed ASP-MLI when driven from binary method is given in Table 3 the maximum possible number of levels in this method is given by;

$$Number\ of\ Levels = 2^{(2N+1)} - 1 \quad (2)$$

Here N is the number of basic blocks of the proposed inverter. Simulation of the proposed cascaded ASP-MLI driven by binary method is simulated using MATLAB/SIMULINK and the results of load voltage and current are shown in Fig. 5.

Proposed Scheme:3 (Multiples of Seven Method): In order to improve the quality of the load voltage further, the DC bus voltages are taken as multiples of seven. The magnitude of DC voltage sources are chose as per the equation (3), and is given below,

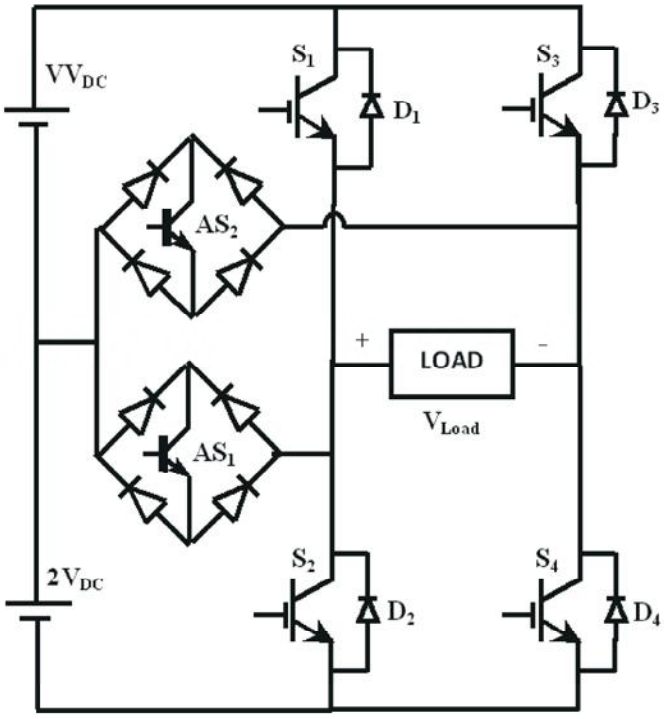


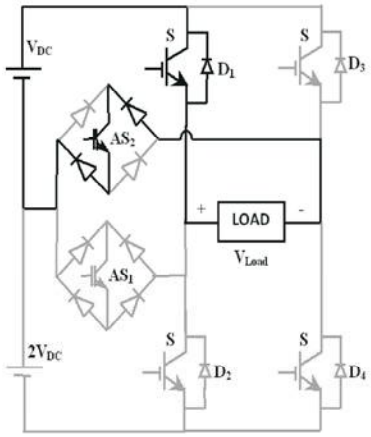
Fig. 1: Basic Block of the proposed Asymmetrical Single-Phase MLI

Table 1: Switching logic of the basic block of the proposed ASP-MLI

Sl.No	S_1	S_2	S_3	S_4	AS_1	AS_2	V_{Load}	Reference
1	ON	OFF	OFF	ON	OFF	OFF	$+3V_{DC}$	Fig 2(e)
2	OFF	OFF	OFF	ON	ON	OFF	$+2V_{DC}$	Fig 2(c)
3	ON	OFF	OFF	OFF	OFF	ON	$+V_{DC}$	Fig 2(a)
4	OFF	OFF	OFF	OFF	ON	ON	0	-
5	OFF	OFF	ON	OFF	ON	OFF	$-V_{DC}$	Fig 2(b)
6	OFF	ON	OFF	OFF	OFF	ON	$-2V_{DC}$	Fig 2(d)
7	OFF	ON	ON	OFF	OFF	OFF	$-3V_{DC}$	Fig 2(f)

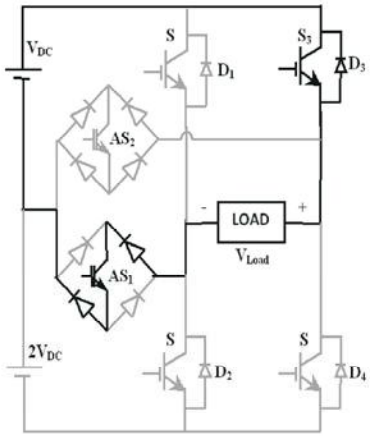
Table 2: Switching Logic of proposed ASP-MLI driven from scheme 1

	Output Voltage of Basic Blocks				Output Voltage of Basic Blocks		
Switching State	1st Basic Block	2nd Basic Block	Load Voltage	Switching State	1st Basic Block	2nd Basic Block	Load Voltage
1	$+2V_{dc}$	$+10\ V_{dc}$	$+12\ V_{dc}$	14	$-V_{dc}$	0	$-\ V_{dc}$
2	$+V_{dc}$	$+10\ V_{dc}$	$+11\ V_{dc}$	15	$-2\ V_{dc}$	0	$-2\ V_{dc}$
3	0	$+10\ V_{dc}$	$+10\ V_{dc}$	16	$+2\ V_{dc}$	$-5\ V_{dc}$	$-3\ V_{dc}$
4	$-\ V_{dc}$	$+10\ V_{dc}$	$+9\ V_{dc}$	17	$+V_{dc}$	$-5\ V_{dc}$	$-4\ V_{dc}$
5	$-2\ V_{dc}$	$+10\ V_{dc}$	$+8V_{dc}$	18	0	$-5\ V_{dc}$	$-5\ V_{dc}$
6	$+2\ V_{dc}$	$+5\ V_{dc}$	$+7\ V_{dc}$	19	$-\ V_{dc}$	$-5\ V_{dc}$	$-6\ V_{dc}$
7	$+\ V_{dc}$	$+5\ V_{dc}$	$+6\ V_{dc}$	20	$-2\ V_{dc}$	$-5\ V_{dc}$	$-7\ V_{dc}$
8	0	$+5\ V_{dc}$	$+5\ V_{dc}$	21	$+2\ V_{dc}$	$-10\ V_{dc}$	$-8V_{dc}$
9	$-\ V_{dc}$	$+5\ V_{dc}$	$+4\ V_{dc}$	22	$+\ V_{dc}$	$-10\ V_{dc}$	$-9\ V_{dc}$
10	$-2\ V_{dc}$	$+5\ V_{dc}$	$+3\ V_{dc}$	23	0	$-10\ V_{dc}$	$-10\ V_{dc}$
11	$+2\ V_{dc}$	0	$+2\ V_{dc}$	24	$-V_{dc}$	$-10\ V_{dc}$	$-11\ V_{dc}$
12	$+\ V_{dc}$	0	$+\ V_{dc}$	25	$-2V_{dc}$	$-10\ V_{dc}$	$-12\ V_{dc}$
13	0	0	0	Magnitude of Voltage Sources	1st Basic Block = V_{dc} ; 2nd Basic Block= $5V_{dc}$		



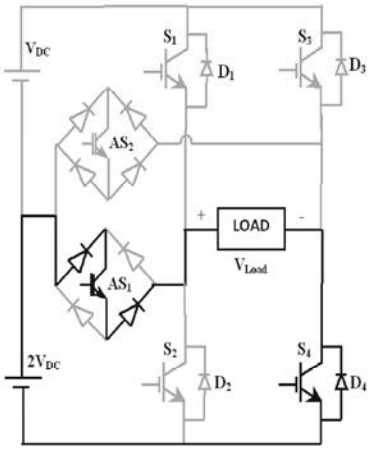
$V_{Load} = + V_{DC}$

Fig. 2 (a)



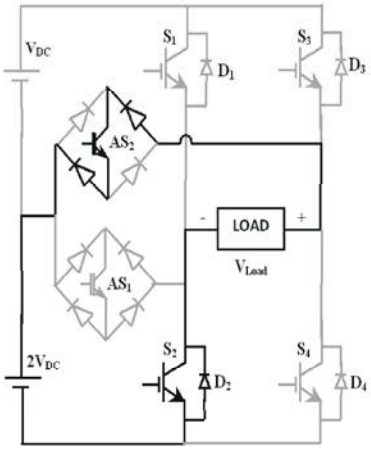
$V_{Load} = - V_{DC}$

Fig. 2 (b)



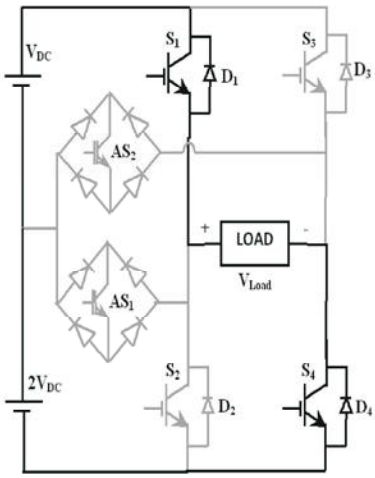
$V_{Load} = +2 V_{DC}$

Fig. 2 (c)



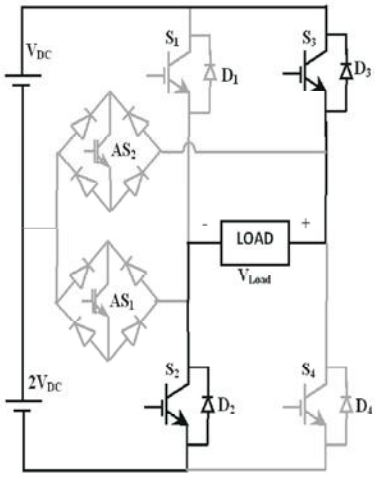
$V_{Load} = - 2V_{DC}$

Fig. 2 (d)



$V_{Load} = +3 V_{DC}$

Fig. 2 (e)



$V_{Load} = - 3V_{DC}$

Fig. 2 (f)

Table 3: Switching Logic of proposed ASP-MLI driven from scheme 2

	Output Voltage of Basic Blocks				Output Voltage of Basic Blocks		
Switching State	1st Basic Block	2nd Basic Block	Load Voltage	Switching State	1st Basic Block	2nd Basic Block	Load Voltage
1	+3 V_{dc}	+12 V_{dc}	+15V_{dc}	17	- V_{dc}	0	- V_{dc}
2	+2 V_{dc}	+12 V_{dc}	+14 V_{dc}	18	-2 V_{dc}	0	-2 V_{dc}
3	+ V_{dc}	+12 V_{dc}	+13 V_{dc}	19	-3 V_{dc}	0	-3 V_{dc}
4	0	+12 V_{dc}	+12 V_{dc}	20	0	-4 V_{dc}	-4 V_{dc}
5	- V_{dc}	+12 V_{dc}	+11 V_{dc}	21	- V_{dc}	-4 V_{dc}	-5 V_{dc}
6	-2 V_{dc}	+12 V_{dc}	+10 V_{dc}	22	-2 V_{dc}	-4 V_{dc}	-6 V_{dc}
7	-3 V_{dc}	+12 V_{dc}	+9 V_{dc}	23	-3 V_{dc}	-4 V_{dc}	-7 V_{dc}
8	0	+8 V_{dc}	+8 V_{dc}	24	0	-8 V_{dc}	-8 V_{dc}
9	- V_{dc}	+8 V_{dc}	+7 V_{dc}	25	- V_{dc}	-8 V_{dc}	-9 V_{dc}
10	-2 V_{dc}	+8 V_{dc}	+6 V_{dc}	26	-2 V_{dc}	-8 V_{dc}	-10 V_{dc}
11	-3 V_{dc}	+8 V_{dc}	+5 V_{dc}	27	-3 V_{dc}	-8 V_{dc}	-11 V_{dc}
12	0	+4 V_{dc}	+4 V_{dc}	28	0	-12 V_{dc}	-12 V_{dc}
13	- V_{dc}	+4 V_{dc}	+3 V_{dc}	29	- V_{dc}	-12 V_{dc}	-13 V_{dc}
14	-2 V_{dc}	+ 4V_{dc}	+2 V_{dc}	30	-2 V_{dc}	-12 V_{dc}	-14 V_{dc}
15	-3 V_{dc}	+4 V_{dc}	+ V_{dc}	31	-3 V_{dc}	-12 V_{dc}	-15 V_{dc}
16	0	0	0	Magnitude of Voltage Sources $V_{DC1} = V_{dc}$; $V_{DC2} = 2V_{dc}$; $V_{DC3} = 4V_{dc}$; $V_{DC4} = 8V_{dc}$;			

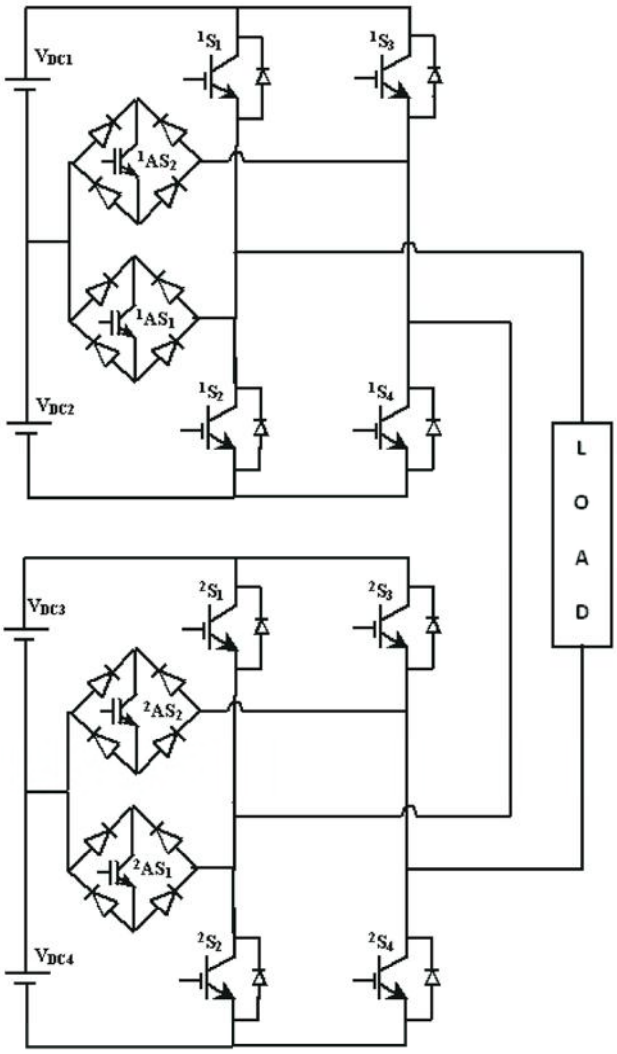


Fig. 3: Cascaded Structure of the Proposed ASP-MLI with two basic blocks

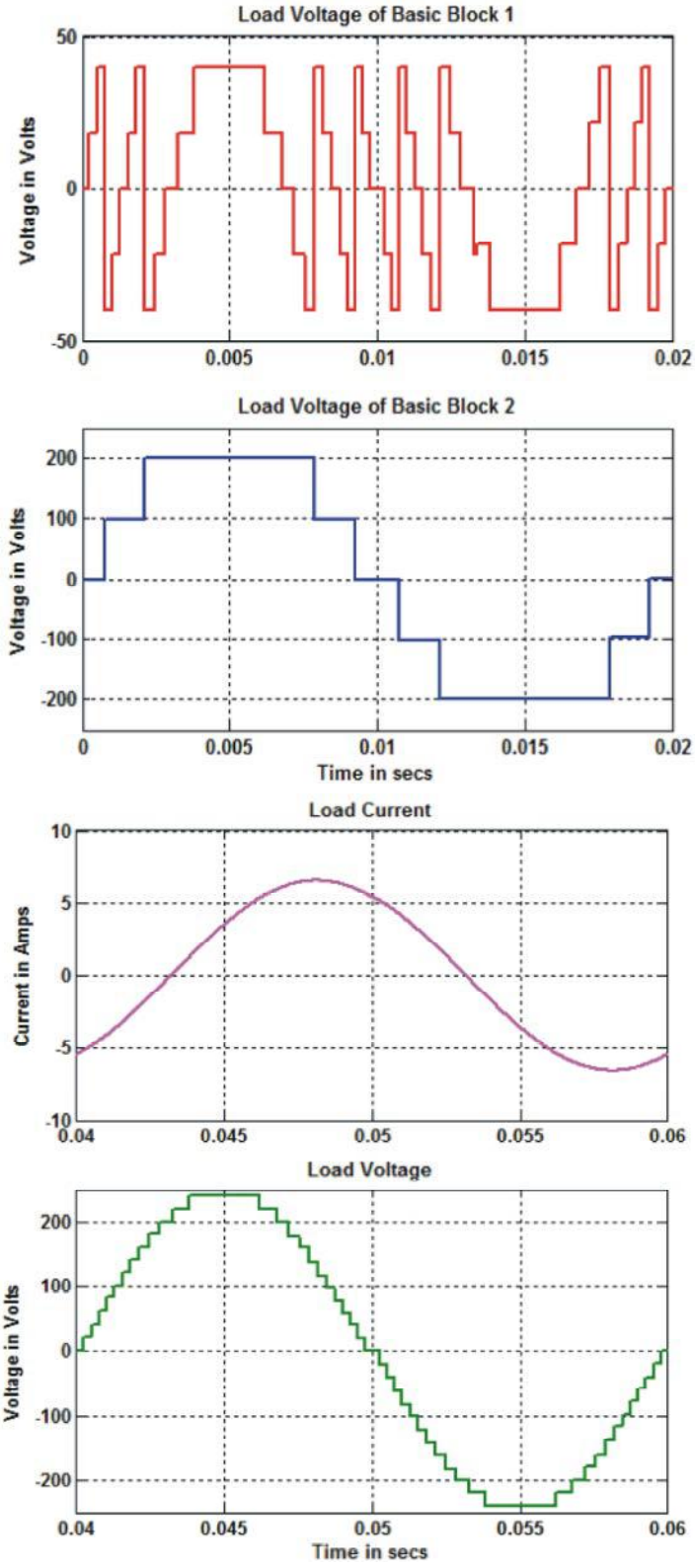


Fig. 4(a): Load Voltage of Basic Block 1 (b) Load Voltage of Basic Block 2 (c) Load Current (d) Load Voltage 25 levels with V_{dc} = 20 Volts

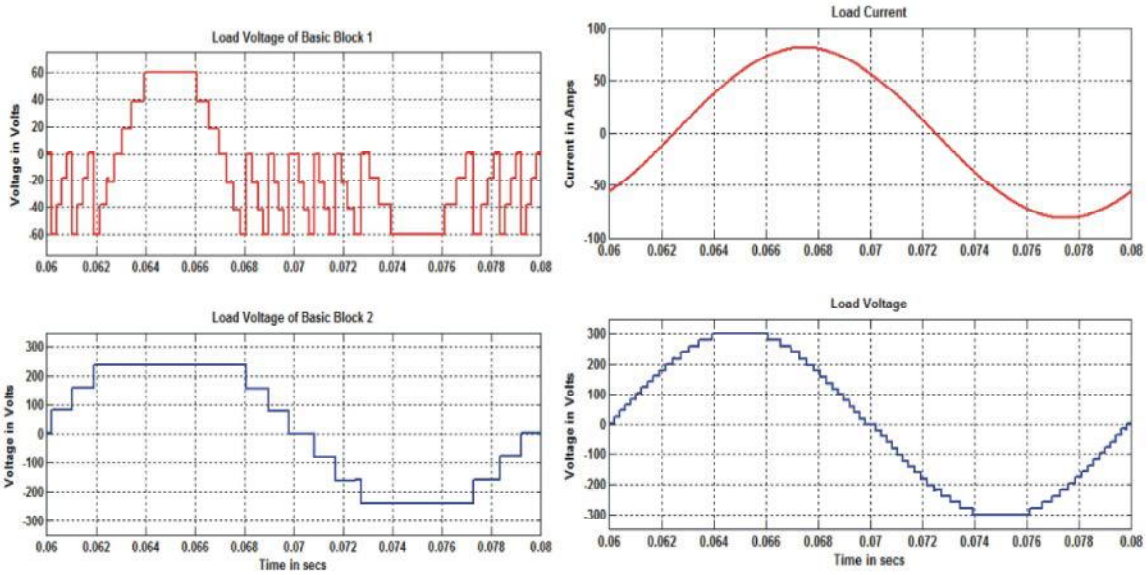


Fig. 5(a): Load Voltage of Basic Block 1 (b) Load Voltage of Basic Block 2 (c) Load Current (d) Load Voltage 31 levels with V_{dc} = 20 Volts

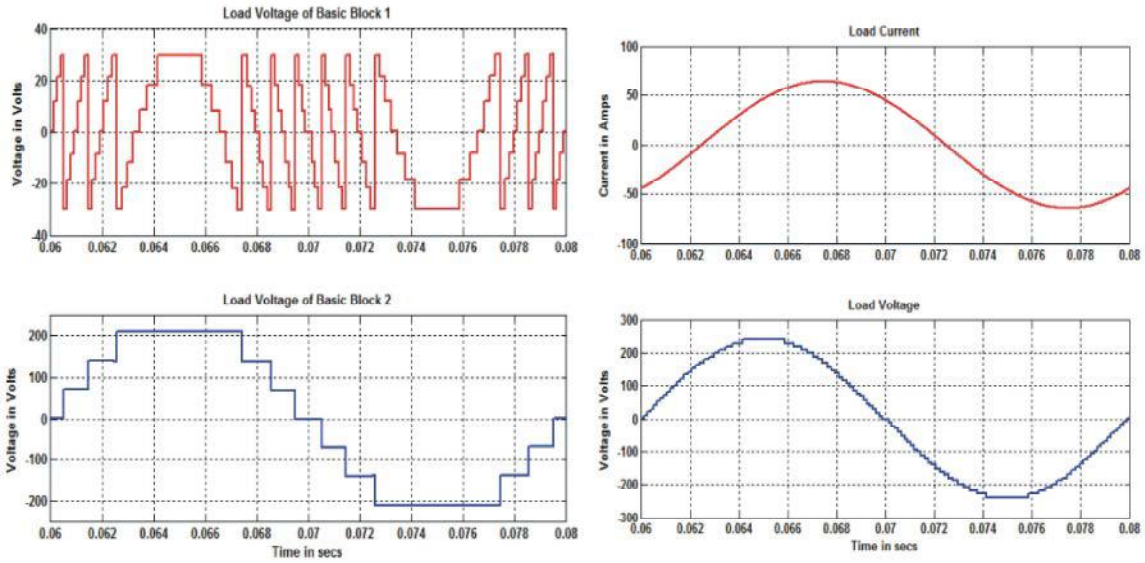


Fig. 5(a): Load Voltage of Basic Block 1 (b) Load Voltage of Basic Block 2 (c) Load Current (d) Load Voltage 49 levels with V_{dc} = 10 Volts

$$V_{DC,n}\begin{cases} 7^{\frac{n-1}{2}} & for\ n:odd \\ 2x7^{\frac{n-2}{2}} & for\ n:evev \end{cases} \quad (3)$$

Here two basic blocks are considered in cascade, hence there are four DC sources in two basic blocks. The magnitude of the four DC sources are taken as;

$V_{DC1} = V_{dc}$, $V_{DC2} = 2V_{dc}$, $V_{DC3} = 7V_{dc}$, $V_{DC4} = 14V_{dc}$

The detailed switching table of the proposed ASMLI when driven from third method is given in Table 4. The maximum possible number of levels in this method is given by;

$$Number\ of\ levels = 7^N \quad (4)$$

Table 4: Switching Logic of proposed ASP-MLI driven from scheme 3

	Output Voltage of Basic Blocks				Output Voltage of Basic Blocks		
Switching State	1st Basic Block	2nd Basic Block	Load Voltage	Switching State	1st Basic Block	2nd Basic Block	Load Voltage
1	$+3V_{dc}$	$+21V_{dc}$	$+24V_{dc}$	26	$-V_{dc}$	0	$-V_{dc}$
2	$+2V_{dc}$	$+21V_{dc}$	$+23V_{dc}$	27	$-2V_{dc}$	0	$-2V_{dc}$
3	$+V_{dc}$	$+21V_{dc}$	$+22V_{dc}$	28	$-3V_{dc}$	0	$-3V_{dc}$
4	0	$+21V_{dc}$	$+21V_{dc}$	29	$+3V_{dc}$	$-7V_{dc}$	$-4V_{dc}$
5	$-V_{dc}$	$+21V_{dc}$	$+20V_{dc}$	30	$+2V_{dc}$	$-7V_{dc}$	$-5V_{dc}$
6	$-2V_{dc}$	$+21V_{dc}$	$+19V_{dc}$	31	$+V_{dc}$	$-7V_{dc}$	$-6V_{dc}$
7	$-3V_{dc}$	$+21V_{dc}$	$+18V_{dc}$	32	0	$-7V_{dc}$	$-7V_{dc}$
8	$+3V_{dc}$	$+14V_{dc}$	$+17V_{dc}$	33	$-V_{dc}$	$-7V_{dc}$	$-8V_{dc}$
9	$+2V_{dc}$	$+14V_{dc}$	$+16V_{dc}$	34	$-2V_{dc}$	$-7V_{dc}$	$-9V_{dc}$
10	$+V_{dc}$	$+14V_{dc}$	$+15V_{dc}$	35	$-3V_{dc}$	$-7V_{dc}$	$-10V_{dc}$
11	0	$+14V_{dc}$	$+14V_{dc}$	36	$+3V_{dc}$	$-14V_{dc}$	$-11V_{dc}$
12	$-V_{dc}$	$+14V_{dc}$	$+13V_{dc}$	37	$+2V_{dc}$	$-14V_{dc}$	$-12V_{dc}$
13	$-2V_{dc}$	$+14V_{dc}$	$+12V_{dc}$	38	$+V_{dc}$	$-14V_{dc}$	$-13V_{dc}$
14	$-3V_{dc}$	$+14V_{dc}$	$+11V_{dc}$	39	0	$-14V_{dc}$	$-14V_{dc}$
15	$+3V_{dc}$	$+7V_{dc}$	$+10V_{dc}$	40	$-V_{dc}$	$-14V_{dc}$	$-15V_{dc}$
16	$+2V_{dc}$	$+7V_{dc}$	$+9V_{dc}$	41	$-2V_{dc}$	$-14V_{dc}$	$-16V_{dc}$
17	$+V_{dc}$	$+7V_{dc}$	$+8V_{dc}$	42	$-3V_{dc}$	$-14V_{dc}$	$-17V_{dc}$
18	0	$+7V_{dc}$	$+7V_{dc}$	43	$+3V_{dc}$	$-21V_{dc}$	$-18V_{dc}$
19	$-V_{dc}$	$+7V_{dc}$	$+6V_{dc}$	44	$+2V_{dc}$	$-21V_{dc}$	$-19V_{dc}$
20	$-2V_{dc}$	$+7V_{dc}$	$+5V_{dc}$	45	$+V_{dc}$	$-21V_{dc}$	$-20V_{dc}$
21	$-3V_{dc}$	$+7V_{dc}$	$+4V_{dc}$	46	0	$-21V_{dc}$	$-21V_{dc}$
22	$+3V_{dc}$	0	$+3V_{dc}$	47	$-V_{dc}$	$-21V_{dc}$	$-22V_{dc}$
23	$+2V_{dc}$	0	$+2V_{dc}$	48	$-2V_{dc}$	$-21V_{dc}$	$-23V_{dc}$
24	$+V_{dc}$	0	$+V_{dc}$	49	$-3V_{dc}$	$-21V_{dc}$	$-24V_{dc}$
25	0	0	0	Magnitude of Voltage Sources $V_{DC1} = V_{dc}$; $V_{DC2} = 2V_{dc}$; $V_{DC3} = 7V_{dc}$; $V_{DC4} = 14V_{dc}$;			

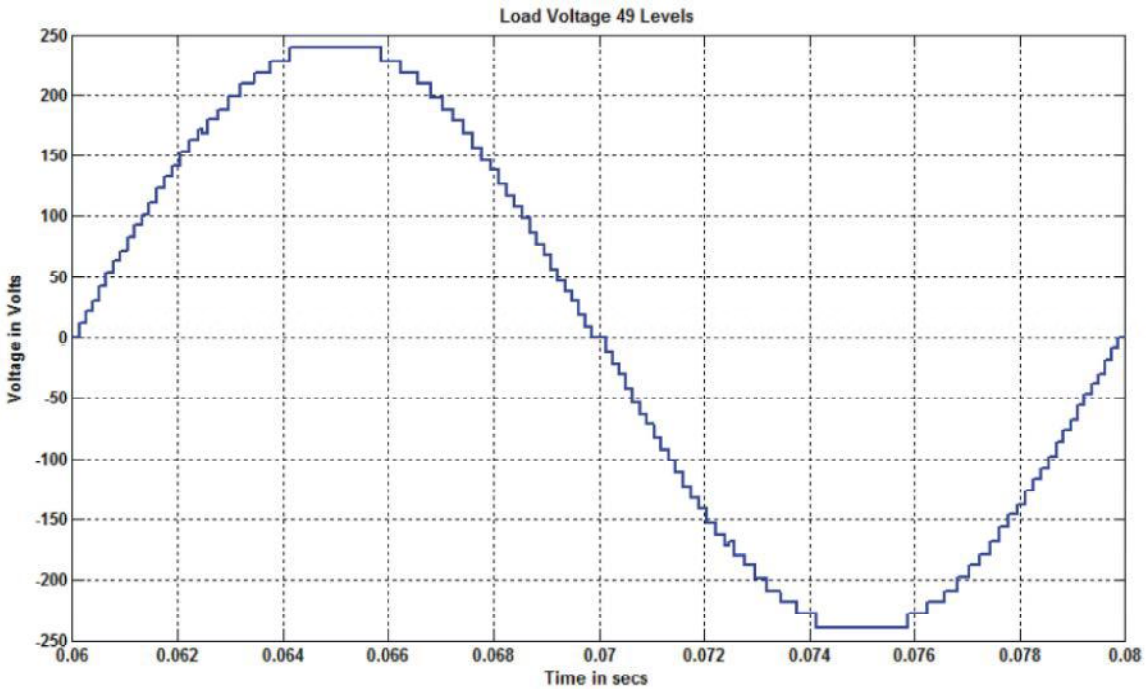
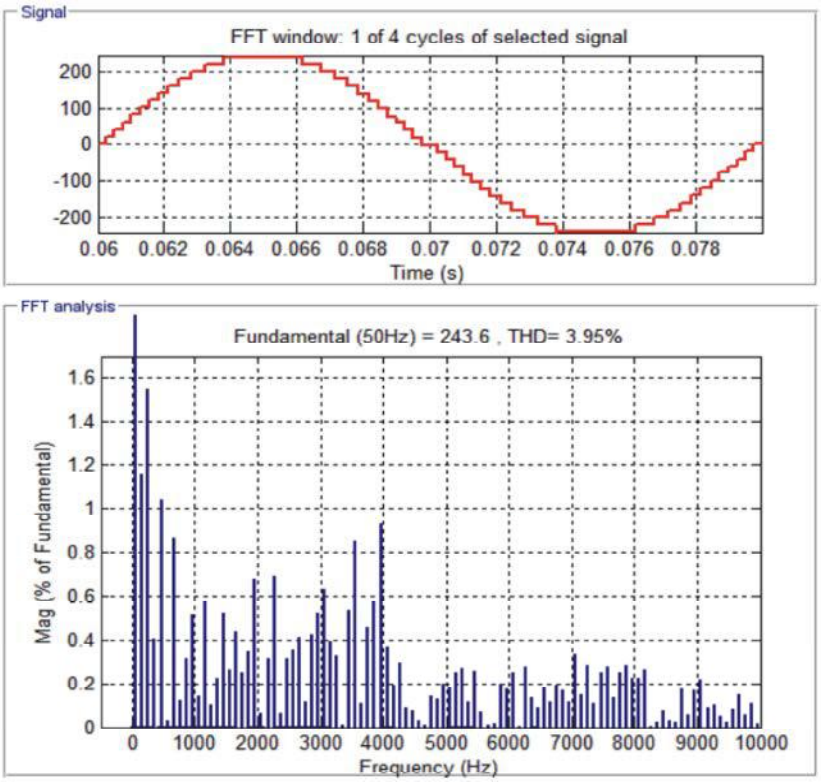
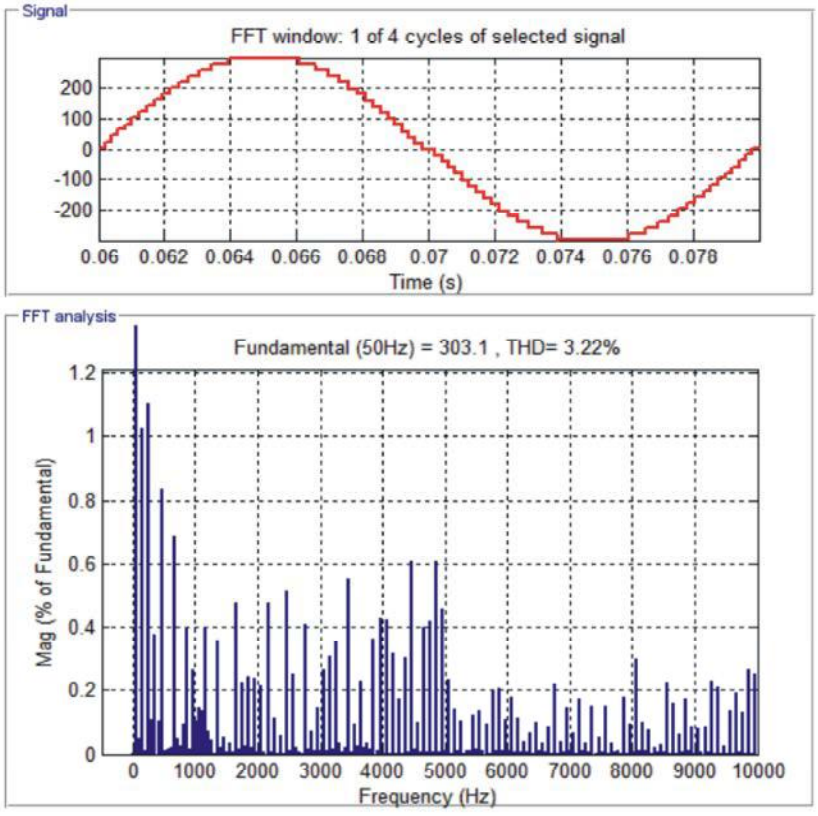


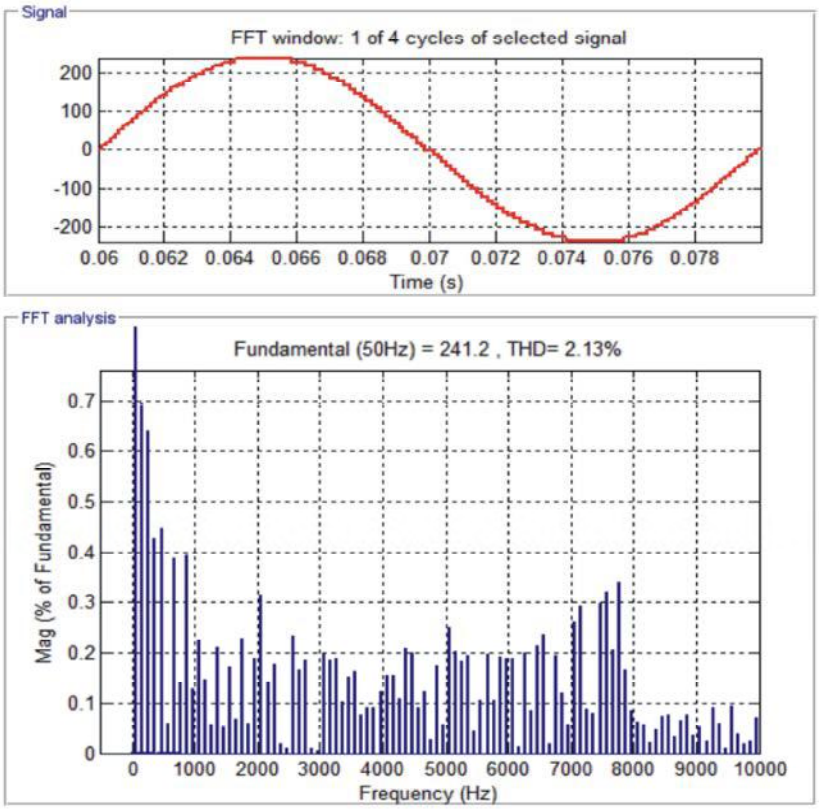
Fig. 6: Enhanced view of the output voltage for 49 level (switching scheme 3)



a. Harmonic Spectrum of Scheme: 1



b. Harmonic Spectrum of Scheme: 2



c. Harmonic Spectrum of Scheme: 3

Fig. 7: Harmonic Spectrum of various schemes

Table 5: Comparison of conventional MLI's with Modified Asymmetrical MLI's

Conventional Asymmetrical MLI's			Modified Asymmetrical MLI's		
Algorithm	No of Power semiconductor	No of output level	Algorithm	No of Power semiconductor	No of output level
1:1:1	4	3	Proposed Scheme:1	6	5
	8	5		12	25
	12	7		18	125
1:2:4	4	3	Proposed Scheme:2	6	5
	8	7		12	31
	12	15		18	127
1:3:9	4	3	Proposed Scheme:3	6	5
	8	9		12	49
	12	27		18	343
	16	81			

Table 6: Comparison of THD value for conventional MLI's with Modified Asymmetrical MLI's

Conventional Asymmetrical MLI's with Basic units		Modified Asymmetrical MLI's with Basic units	
Algorithm	THD Value	Algorithm	THD Value
1:1	19.17 %	Proposed Scheme:1	3.95 %
1:2	13.86 %	Proposed Scheme:2	3.22 %
1:3	10.70 %	Proposed Scheme:3	2.13 %

Here N is the number of basic blocks of the proposed inverter. Simulation of the proposed cascaded ASMLI driven by third method is simulated using MATLAB/ SIMULINK and the results of load voltage and current are shown in Fig. 6. Fig. 6 shows the enhanced view of the output voltage for 49 levels (switching scheme 3).

Section III: Comparison of Various Proposed Schemes of Asymmetrical Multilevel Inverter: In the modified Asymmetrical Multilevel inverter, the number power semiconductor switches required are less compared to conventional asymmetrical multilevel inverter to produce the output voltage with improved THD value. Fig. 7 shows the harmonic spectrum of various schemes with the representation of THD levels in each of the scheme. The Table 5 gives the comparison of switching devices used in proposed ASP-MLI with the conventional MLI's with respect to number of output levels. The Table 6 give the comparison of THD levels in ASP-MLI with the conventional MLI's.

CONCLUSION

In this paper, a novel modified Asymmetrical Single-Phase Multilevel Inverter (ASP-MLI) topology has been was proposed. The proposed topology has superior features compared with the conventional MLI's in terms of the power semiconductor switches. In this MLI, three switching schemes were proposed. The first switching scheme is capable of producing 25 levels, second switching scheme produces 31 levels and the third scheme produces 49 levels at the output voltage. All the switching schemes were simulated in MATLAB/ SIMULINK environment and the results were presented. The THD levels of the proposed schemes are within the specified limits of IEEE 519 standards. The proposed ASMLI can be used in grid connected renewable energy applications.

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