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Single-phase fifteen-level grid-connected inverter for photovoltaic system with evolutionary programming based MPPT algorithm

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Abstract

This paper presents a new single phase grid connected cascaded multilevel inverter with minimum number of switches for photovoltaic (PV) based power conversion systems along with Evolutionary Programming (EP) based Maximum Power Point Tracking (MPPT) algorithm. The projected inverter can output more number of voltage levels with minimum number of switching devices. The number of gate driving circuit is reduced, which leads to the diminution of size and power consumption in the driving circuits. The THD of the output waveform is reduced. The proposed inverter is driven by the mixture modulation technique. In this paper, the circuit configuration, theoretical operation and simulation results with MATLAB/SIMULINK are also shown. The EP based MPPT is capable of extracting maximum power from the PV array.

Keywords: Cascaded H-bridge inverter (CHB); Hybrid modulation (HM); Evolutionary Programming (EP); Maximum Power Point Tracking (MPPT)

1. Introduction

Recently, non conventional energy resources have been attractive sources of energy due to the escalating energy consumption, exhausting fossil fuels and their impact on environment issues. This makes a significant contribution in the research of renewable energy sources (Bayod-Rujula et al., 2013; Merei et al., 2013; Askarzadeh, 2013a,b). Among the clean and green power sources, the photovoltaic (PV) solar energy comes up as being a very interesting alternative to supplement the generation of electricity, because it offers many advantages such as fuel cost is nil, low maintenance, noise free due to the absence of rotating parts and they do not generate any contaminated or dangerous gases that pollute the environment (Jung and Ahmed, 2012; Abusorrah et al., 2013).

PV system converts solar energy directly into electricity. Power generated from PV sources can be delivered to electrical grid through inverters. A single-phase grid-connected inverter is typically used for low-power applications whose requirement is less than 10 kW (e.g. residential applications) (Ahmad et al., 2013). Full-bridge three-level inverter topologies are commonly used in such applications. The desired specifications as per IEEE standards can be achieved by switching power electronic devices of the three-level inverter at very high frequency. But, this leads

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to increased switching losses, acoustic noise, and level of interference to other equipments. These drawbacks significantly reduce the overall efficiency of the PV system. Improved output waveform at the inverter terminals reduces its total harmonic content, which in turn reduces the size of the filter and the level of electromagnetic interference (EMI) due to inverter's switching operation (Fernão Pires et al., 2012; Letting et al., 2012).

Multilevel inverters are appropriate options for realizing the desired specifications as per standards (Tsengenes and Adamidis, 2011; Calais et al., 1999; Beser et al., 2010). Various topologies of multilevel inverter have been investigated in the literature. The most common types among them are the diode clamped (Jaime Alonso-Martinez et al., 2010), the flying capacitor (Ravi et al., 2011; Jaime Alonso-Martinez et al., 2010), the Cascaded H-bridge (Valan Rajkumar and Manoharan, 2013; Malinowski et al., 2010), the full bridge with cascaded transformers (Feel-soon Kang et al., 2005) and modified H-bridge multilevel inverters (Hinago and Koizumi, 2010; Fernão Pires et al., 2012).

Among the various types of multilevel inverter, cascaded type has been gaining importance in particular for grid-connected PV applications for the following reasons

1. The output voltage level required for grid power injection can be achieved without the use of a transformer as the voltage boosting is shared between the dc series connection of PV modules and the cascade connection of H-bridge outputs.
2. Like other multilevel inverter topologies, the CHB-MLI allows the synthesis of staircase ac output waveforms with lower total harmonic distortion (THD) compared to those generated by three-level-based inverters, thus releasing output filter requirements for the compliance of grid harmonic standards (Malinowski et al., 2010). Depending on the operation power level, this synthesis can be carried out either at the fundamental frequency or at higher switching frequencies using multicarrier-based modulations (Liu et al., 2009).
3. This topology allows the connection of independent strings of PV modules to the input dc links of the power stage. Since the dc link voltages can be independently controlled, the maximum power extraction of a reduced number of PV modules can be accomplished with the help of Maximum Power Point Tracking (MPPT) algorithms. This improves both PV system reliability and energy production when the PV modules operate under mismatching conditions such as in the case of partial shadowing (Liu et al., 2009; Rodríguez et al., 2002; McGrath and Holmes, 2002)

This paper proposes a novel modified Cascaded H-bridge single-phase multilevel inverter with bridge rectifier embedded bidirectional power semiconductor device and a novel hybrid pulse width modulation (HPWM) technique. The topology is extended to a grid-connected photovoltaic system with EP based maximum-power-point tracking algorithm (EP-MPPT) and a current-control algorithm.

2. Proposed multilevel inverter configuration

The proposed single-phase fifteen-level inverter is the revised edition of the inverter developed in (Hinago and Koizumi, 2010). It comprises two H-bridge inverters connected in cascade. The upper H bridge inverter is conventional, where as the lower H bridge inverter is the one developed in (Rahim et al., 2010). Fig. 1 shows the circuit topology of the proposed multilevel inverter. The modified H-bridge configuration is extensively advantageous over other configurations, i.e., less number of power switches, power diodes, capacitors and isolated DC sources.

Separate PV arrays are connected to the upper and lower H bridge inverter through individual dc–dc boost converter. The upper H-bridge is fed from one PV array and the lower H-bridge is fed from six PV arrays connected in series. The dc–dc boost converter is used to boost up the low voltage output of the PV array to the level required by the grid. High dc bus voltages are essential to make sure that power flows from the PV arrays to the grid. A filtering inductance L_f is used to filter the current injected into the grid. Switches SW_1 and SW_2 are used to disconnect the PV power generation system from the grid during islanding operation. The load is placed between switches SW_1 and SW_2. By switching the inverter properly, it can produce fifteen output voltage levels from the DC supplies.

2.1. Operation of the proposed fifteen level inverter

The proposed multilevel inverter is of asymmetrical type. The magnitude of each DC link capacitor in the lower H-bridge is two times the magnitude of the upper H bridge capacitor. (i.e. $V_{dc2} = V_{dc3} = V_{dc4} = 2V_{dc1}$). Hence, the DC link voltage of the lower H bridge is six times the DC link voltage of the upper H bridge (i.e. $V_{dc,low} = 6V_{dc1}$). Owing to this, the upper H bridge inverter is fed from a single PV array, where as the lower H-bridge inverter is fed from six series connected PV arrays. Thus 90% of the power fed to the load is from the lower inverter and the upper inverter supplies only 10%. The upper H bridge inverter is a conventional inverter which generates three level output (i.e. $+V_{dc1}$, 0, $-V_{dc1}$). The lower H bridge inverter is capable of generating seven level output (i.e. $+6V_{dc1}$, $+4V_{dc1}$, $+2V_{dc1}$, 0, $-2V_{dc1}$, $-4V_{dc1}$, $-6V_{dc1}$). The lower H bridge inverter operation can be divided into seven switching states, as shown in Fig. 2(a)–(g).

Fig. 2(a) and (g) are switching sequences of the lower inverter in the conventional mode. Fig. 2(b), (c), (e) and (f) show the additional switching sequence of the lower H bridge. The combined switching combinations of the upper and lower H bridge inverter to develop fifteen levels at the load terminals are given in Table 1.

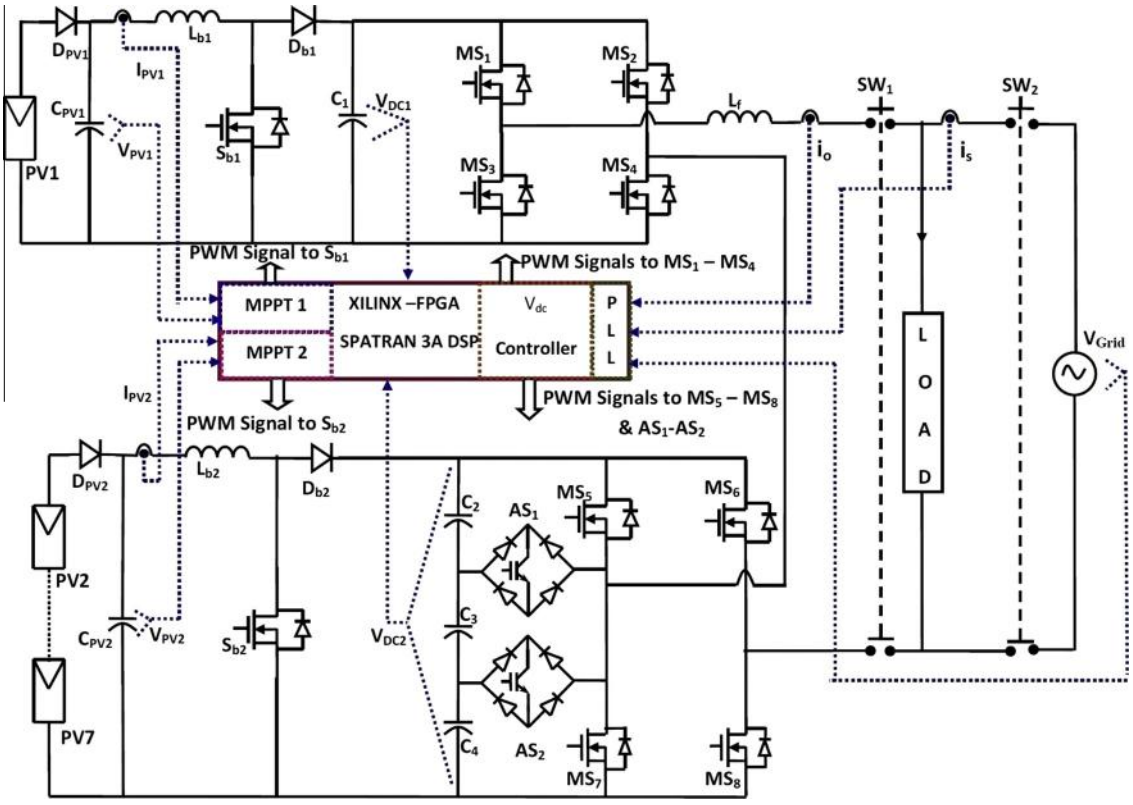

Fig. 1. Proposed single-phase 15-level grid-connected for photovoltaic systems.

2.2. Hybrid PWM modulation scheme

In order to reduce the switching losses in the proposed inverter, hybrid PWM modulation technique is used (Jie Zhang et al., 2001). Since most of the power fed to the load is from the lower inverter, the switches of the lower H bridge inverter are switched at low frequency (i.e. at fundamental frequency, 50 Hz). Whereas, the upper H bridge inverter switches are switched at high frequency (i.e. at 10 kHz). Fig. 3 shows the upper, lower and load voltage waveforms of the proposed inverter. In Fig. 3(b), the dotted waveform indicates the reference waveform of the upper inverter. In order to derive the voltage waveform as shown in Fig. 3, the switching signals are derived mathematically by using simple arithmetic and logical operations. The total reference waveform is given as

$$V_{ref} = \sin(\omega t) \tag{1}$$

The reference waveform of the upper inverter is generated by using the following expressions,

$$\text{ZCD} = \begin{cases} 1 & \text{if} \quad V_{ref} > 0 \\ 0 & \text{if} \quad V_{ref} < 0 \end{cases} \tag{2}$$

where ZCD means Zero Crossing Detector.

The expected lower inverter voltage is given as

$$V_{LOW,Expected} = \left(round\left(\frac{|V_{ref}|}{0.4}\right) * 0.4 * Z_1\right) + \left(round\left(\frac{|V_{ref}|}{-0.4}\right) * 0.4 * \overline{Z}_1\right) \tag{3}$$

$$V_{up,ref} = 7 * \left(V_{ref} - V_{LOW,Expected}\right) \tag{4}$$

Expression (4) is the one which produces reference waveform of the upper inverter as shown in Fig. 3(b). The reference signal generated from expression (4) is compared with triangular carrier of 10 kHz and the comparator output is given to the switches MS_1 and MS_3 of the upper inverter. Similarly, Eq. (4) is subtracted from one, to get another reference and that is again compared with high frequency carrier. This compared output is used to drive the switches MS_2 and MS_4 of the upper inverter. In order to generate switching patterns for the lower inverter, the first step is to generate the reference waveform for the lower inverter

$$V_{low,ref} = round\left(\frac{|V_{ref}|}{0.4}\right) \tag{5}$$

The next step is to split the above reference signal into three (i.e. R_1, R_2 and R_3) and they are given as,

$$R_1 = \begin{cases} 1 & \text{if} \quad V_{low,ref} > 1 \\ 0 & \text{if} \quad V_{low,ref} < 0 \end{cases} \quad R_2 = \begin{cases} 1 & \text{if} \quad V_{low,ref} > 2 \\ 0 & \text{if} \quad V_{low,ref} < 0 \end{cases} \quad R_3 = \begin{cases} 1 & \text{if} \quad V_{low,ref} > 3 \\ 0 & \text{if} \quad V_{low,ref} < 0 \end{cases} \tag{6}$$

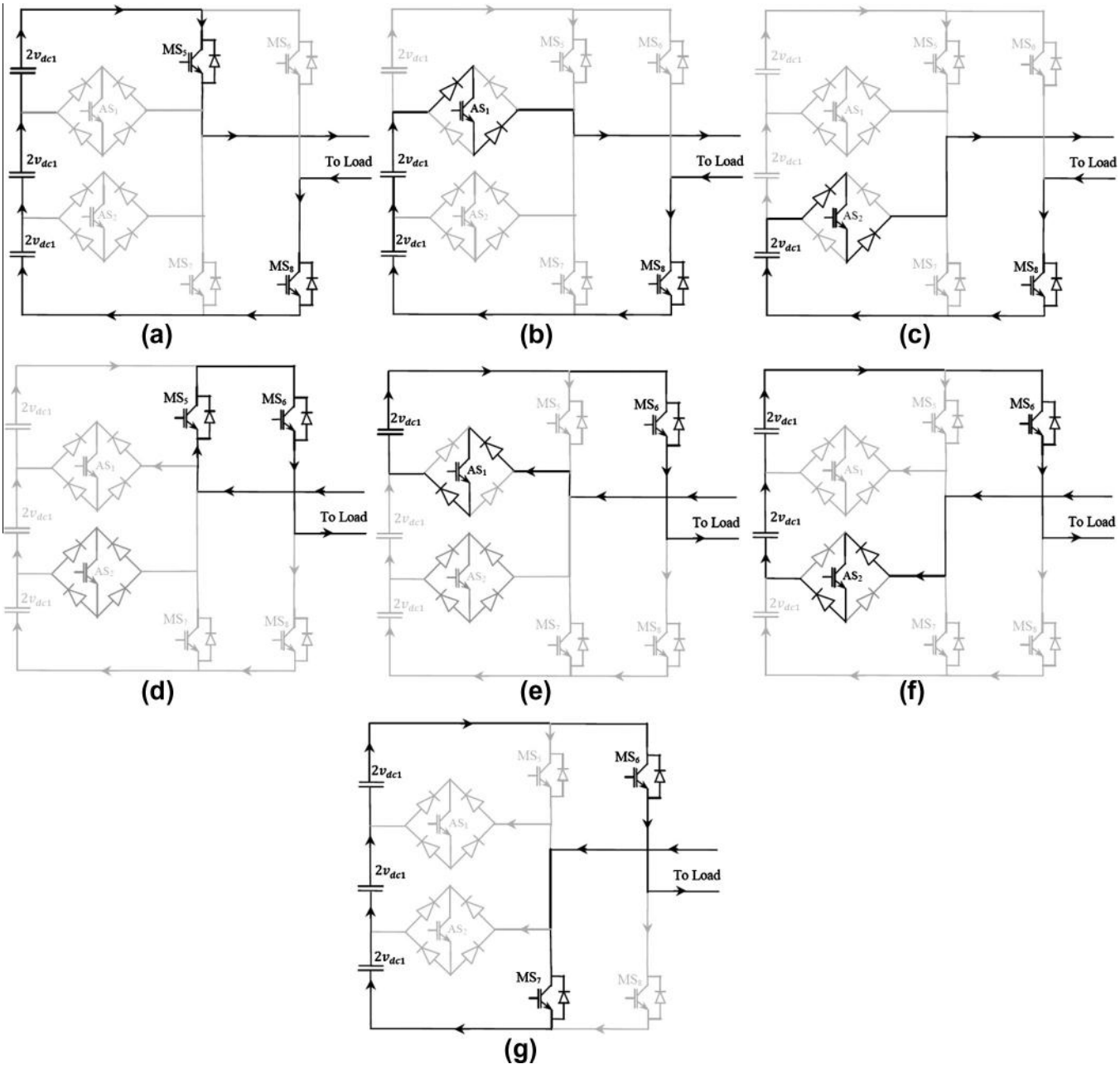

Fig. 2. Switching combinations required to generate output voltage of lower H bridge inverter (a) $V_{low} = 6V_{dc1}$, (b) $V_{low} = 4V_{dc1}$, (c) $V_{low} = 2V_{dc1}$, (d) $V_{low} = 0$, (e) $V_{low} = -2V_{dc1}$, (f) $V_{low} = -4V_{dc1}$, (g) $V_{low} = -6V_{dc1}$.

The main switches of the lower inverter are switched as per the equations given below

$$MS_5(t) = [(\overline{R}_1) + (R_3)] * Z_1 \quad (7)$$

$$MS_6(t) = [(\overline{R}_1) * (\overline{Z}_1)] + [(\overline{R}_1) * (Z_1)] \quad (8)$$

$$MS_7(t) = [(\overline{R}_1) + (R_3)] * \overline{Z}_1 \quad (9)$$

$$MS_8(t) = [(R_1) * (Z_1)] + [(\overline{R}_1) * (\overline{Z}_1)] \quad (10)$$

where + denotes logical OR operation and * denotes multiplication of signals. The switching patterns of auxiliary switches AS_1 and AS_2 are

$$AS_1(t) = ((R_1 \oplus R_2) * \overline{Z}_1) + ((R_2 \oplus R_3) * Z_1) \quad (11)$$

$$AS_2(t) = ((R_1 \oplus R_2) * Z_1) + ((R_2 \oplus R_3) * \overline{Z}_1) \quad (12)$$

where $\oplus$ denotes XOR operation. Eqs. (4), (7)–(11), (and) (12) are used to generate switching patterns for all the switches of the proposed inverter.

2.3. MPPT algorithm for PV cells using evolutionary programming

The power generated from a given PV module mainly depends on solar irradiance and temperature. As these

Table 1
Switching combinations of the proposed inverter.

Upper H bridge switches (high frequency switches)				Lower H bridge switches (low frequency switches)						Mode	Output load voltage $V_{dc2} = V_{dc3} = V_{dc4} = 2V_{dc1}$		
MS_1	MS_2	MS_3	MS_4	MS_5	MS_6	MS_7	MS_8	AS_1	AS_2		V_{up}	V_{low}	$V_{total} = V_{up} + V_{low}$
ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	I	$0 \leftrightarrow V_{dc1}$	$6V_{dc1}$	$6V_{dc1} \leftrightarrow 7V_{dc1}$
OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	II	$-V_{dc1} \leftrightarrow 0$	$6V_{dc1}$	$5V_{dc1} \leftrightarrow 6V_{dc1}$
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	III	$0 \leftrightarrow V_{dc1}$	$4V_{dc1}$	$4V_{dc1} \leftrightarrow 5V_{dc1}$
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	IV	$-V_{dc1} \leftrightarrow 0$	$4V_{dc1}$	$3V_{dc1} \leftrightarrow 4V_{dc1}$
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	V	$0 \leftrightarrow V_{dc1}$	$2V_{dc1}$	$2V_{dc1} \leftrightarrow 3V_{dc1}$
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	VI	$-V_{dc1} \leftrightarrow 0$	$2V_{dc1}$	$V_{dc1} \leftrightarrow 2V_{dc1}$
ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	VII	$0 \leftrightarrow V_{dc1}$	0	$0 \leftrightarrow V_{dc1}$
OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	VIII	$0 \leftrightarrow -V_{dc1}$	0	
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	IX	$V_{dc1} \leftrightarrow 0$	$-2V_{dc1}$	$-V_{dc1} \leftrightarrow -2V_{dc1}$
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	X	$0 \leftrightarrow -V_{dc1}$	$-2V_{dc1}$	$-2V_{dc1} \leftrightarrow -3V_{dc1}$
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	XI	$V_{dc1} \leftrightarrow 0$	$-4V_{dc1}$	$-3V_{dc1} \leftrightarrow -4V_{dc1}$
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	XII	$0 \leftrightarrow -V_{dc1}$	$-4V_{dc1}$	$-4V_{dc1} \leftrightarrow -5V_{dc1}$
ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	XIII	$V_{dc1} \leftrightarrow 0$	$-6V_{dc1}$	$-5V_{dc1} \leftrightarrow -6V_{dc1}$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	XIV	$0 \leftrightarrow -V_{dc1o}$	$-6V_{dc1}$	$-6V_{dc1} \leftrightarrow -7V_{dc1}$

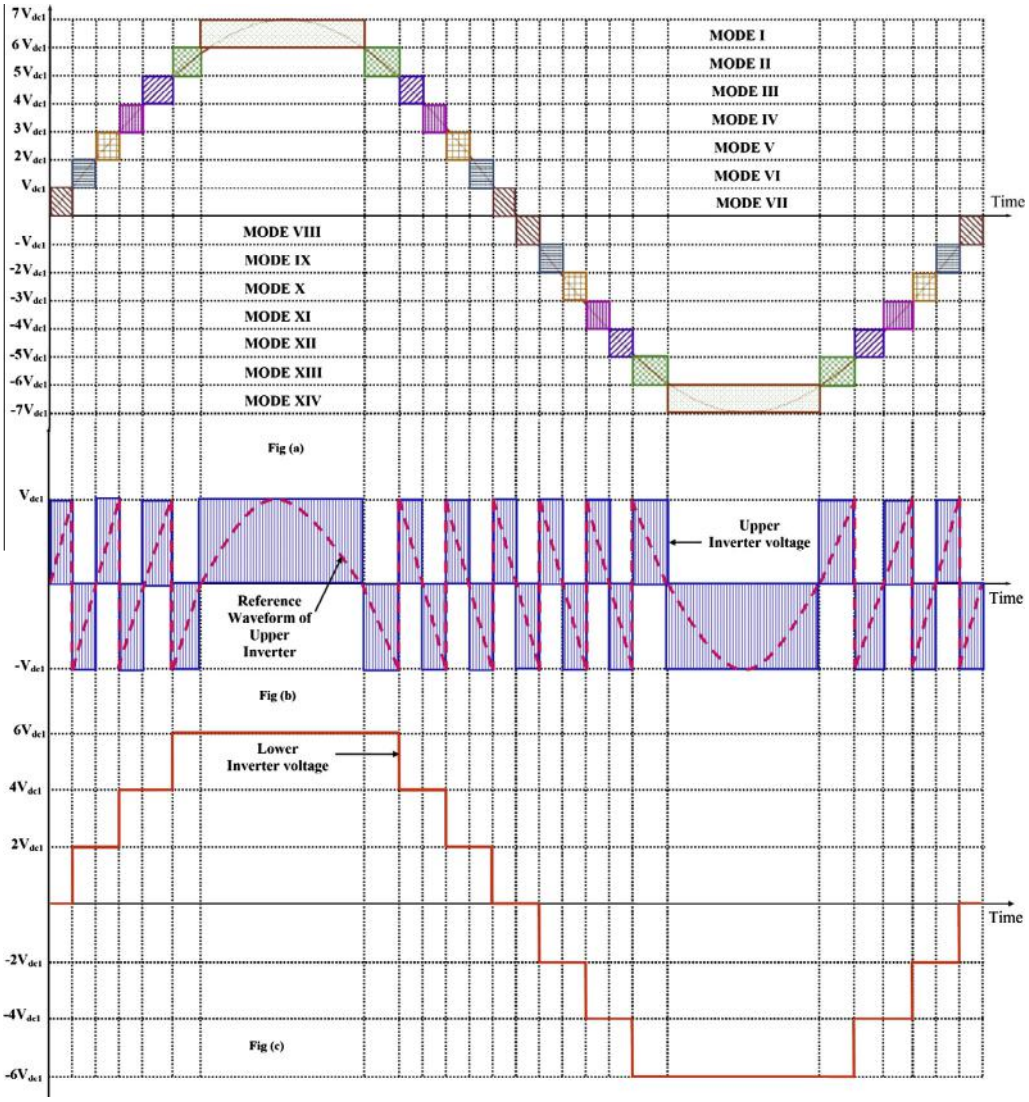

Fig. 3. (a) Load voltage waveform with fourteen modes of operation, (b) upper inverter voltage with reference waveform, (c) lower inverter voltage.

quantities vary with time, it is necessary to develop a control logic that continuously monitors the terminal voltage and current and updates the control signal accordingly. Furthermore, for optimal operation of a PV module, its terminal voltage must be equal to the corresponding Maximum Power Point (MPP) value (Heydari-doostabad et al., 2013; Li et al., 2013; Lalili et al., 2013; Roshan and Moallem, 2013). In this paper, an attempt is made to make use of the Evolutionary Programming (EP) technique to track the maximum power point. EP is an artificial intelligence method based on the mechanics of natural selections–mutation, competition and evolution. The objective function to determine MPP is derived from the basic single diode model of PV cell (Caisheng wang, 2006; Ghani et al., 2013; Siddiqui et al., 2013; Lun et al., 2013). The voltage–current relations for single diode model is

$$I = I_L - I_0\left(\exp\left[\left(\frac{q}{\gamma k T_C}\right)\times(V+IR_s)\right]-1\right) \quad (13)$$

where I_L is the light current, which is a function of irradiation and cell temperature, I_0 is the reverse saturation current of the diode, q is the electron charge constant, k is the Boltzmann constant, T_c is the cell temperature, I and V are the current and voltage at the terminals of the PV array. The expressions of I_L and I_0 are dealt in detail in (Caisheng wang, 2006; Lun et al., 2013). The power output of the PV array can be obtained by multiplying Eq. (13) with V, which results in

$$P = \left[I_L - I_0\left(\exp\left[\left(\frac{q}{\gamma k T_C}\right)\times(V+IR_s)\right]-1\right)\right]\times[V] \quad (14)$$

In the above expression substituting V_{MAX} instead of V and I_{MAX} instead of I, gives the expression for P_{MAX}. The P_{MAX} expression is taken as the objective function, which is maximized by using EP algorithm. The parameters of PV panels used in the simulation and experimental setup are given in Table 2. The results of the EP based MPPT algorithm is compared with that of the experimental results and the simulated values. The results of the comparison are tabulated in Table 3.

2.3.1. Detailed algorithm steps

2.3.1.1. Initialization. The initial control variable population is selected by randomly selecting

$$p_i = [I^i_{pv}, V^i_{pv}] \quad \text{where } i = 1, 2, 3 \ldots m.$$

Table 2
Parameters of PV panel.

Parameter	Value
Short circuit current at reference condition I_{sc}	5.48 A
Open circuit voltage at reference condition V_{oc}	43.6 V
MPP voltage at reference condition V_{mp}	35.8 V
MPP current at reference condition I_{mp}	5.03 A
Series resistance R_s	0.1133 Ω
Irradiance at standard test conditions (STC)	1000 W/m^2
Cell temperature at standard test conditions	25 °C
Maximum power @ STC	180 W

where m is the population size, from the sets of uniform distribution ranging over $[I^{min}(0), I^{max}(I_{SC}$ at STC)] and $[V^{min}(0), V^{max}(V_{oc}$ at STC)]. The fitness score f_i of each p_i is calculated by using the expression,

$$f_i = P = \left[I_L - I_0\left(\exp\left[\left(\frac{q}{\gamma k T_C}\right)\times(V_{pv}+I_{pv}R_s)\right]-1\right)\right]\times[V_{pv}] \quad (14a)$$

2.3.1.2. Mutation. Each p_i is muted and assigned to p_{i+m} in accordance with the following expression,

$$p_{i+m,j} = p_{i,j} + N\left(0, \beta(x_{j\max} - x_{j\min})\frac{f_i}{f_{\max}}\right), \quad i = 1, 2, \ldots n$$

where $p_{i,j}$ denotes the j^{th} element of the i^{th} individual; $N(\mu, \sigma^2)$ represents the Gaussian random variable with mean μ and variance σ^2; f_{max} is the maximum fitness function of the old generation which is obtained in statistics; $x_{j\max}$ and $x_{j\min}$ are the maximum and minimum limits of the j^{th} element; β is the mutation scale which is given as $0 \leqslant \beta \leqslant 1$. If any $p_{i+m,j}$, $j = 1, 2, \ldots, n$, where n is the number of control variables, exceeds its limits, $p_{i+m,j}$ will be the limit value. The corresponding fitness is obtained again by using (14a). A combined population is formed with the old generation and the mutated old generation.

2.3.1.3. Competition. Each individual p_i in the combined population has to compete with some other individuals based on the maximum fitness value (i.e. PV Panel Power) to get its chance to be transcribed to the next generation.

2.3.1.4. Determination. The convergence of fitness function is checked. If the convergence condition is not met, the Mutation and Competition processes will run again. If it converges the program stops.

2.4. Design of circuit elements of the proposed grid connected inverter

The desired specification of the grid is 230 V (RMS) @ 50 Hz. Hence the proposed inverter also has to supply 230 V (RMS) @ 50 Hz. In the proposed inverter, the upper inverter is supplied from one PV module and the lower inverter is fed from six PV modules. So the total 230 V (RMS) has to be supplied by these seven modules. Thus the desired output of the upper boost converter is given by,

$$V_{DC1} = \frac{230 * \sqrt{2}}{7} = 46.47 \text{ Volts} \quad (15)$$

The desired output of the lower boost converter is given by,

$$V_{DC2} = [230 * \sqrt{2}] - 46.47 = 278.8 \text{ Volts} \quad (16)$$

2.4.1. Design of upper boost converter

Since the upper DC/DC boost converter is connected one PV module, the input voltage (V_{in}) of the upper boost

Table 3
Summary of MPP results.

Weather conditions temp = 25 °C	Experimental MPP			Evolutionary programming (EP) MPP			Simulation MPP		
Irradiance W/m^2	V_{mp} [V]	I_{mp} [A]	P_{mp} [W]	V_{mp} [V]	I_{mp} [A]	P_{mp} [W]	V_{mp} [V]	I_{mp} [A]	P_{mp} [W]
1000	35.8	5.03	180.0	35.34	5.10	180.05	35.56	5.06	181.11
800	34.84	4.07	141.82	34.79	4.08	141.88	35.09	4.04	141.94
600	34.18	3.05	104.18	34.07	3.06	104.21	34.40	3.03	104.28
400	33.12	2.03	67.28	33.01	2.04	67.32	33.40	2.02	67.38
200	31.24	1.01	31.68	31.12	1.02	31.73	31.71	1.00	31.79

converter is approximately 35.8 Volts at 1 kW/m^2 and 31.12 Volts at 200 W/m^2 (assuming that the minimum irradiance at the installed location). From (15) the output (V_{out}) of the upper boost converter should be equal to 46.47 Volts. The relationship between input voltage and output voltage of boost converter in terms of duty cycle is given by,

$$V_{out} = \frac{V_{in}}{1-D} \tag{17}$$

So the maximum and minimum duty cycle is given by,

$$\left.\begin{aligned} D_{\max} &= 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{31.12}{46.47} = 0.33 \quad (18a) \\ D_{\min} &= 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{35.80}{46.47} = 0.23 \quad (18b) \end{aligned}\right\} \tag{18}$$

Limit of duty cycles is 0.23–0.33. The duty cycle is not fixed due to the tracking process of the maximum power point voltage. In the above expression the worst condition is the minimum input voltage condition, thus Eq. (18a) is taken into consideration for further designing.

(a) ***Inductor design:***

The value of the inductor used in the upper boost converter is determined as,

$$L_{b1} = \frac{V_{in} * (V_{out} - V_{in})}{(\Delta I_L) * f_s * V_{\text{out}}} \tag{19}$$

where ΔI_L is the ripple value of inductor current and f_s is the switching frequency boost converter. The value of ΔI_L can be calculated as follows,

$$\Delta I_L = (2\% \text{ to } 4\%) * I_{out(\max)} * \frac{V_{out}}{V_{in}} \tag{20}$$

$$\Delta I_L = (0.03) * 5.03 * \frac{46.47}{31.12} = 0.23 \text{ A}$$

where $I_{out(\max)}$ is the maximum current delivered from the PV module under maximum irradiance conditions (i.e. at 1 kW/m^2).

Therefore the value of inductance can be calculated as,

$$L_{b1} = \frac{V_{in} * (V_{out} - V_{in})}{(\Delta I_L) * f_s * V_{out}} = \frac{31.12 * (46.47 - 31.12)}{0.23 * 4000 * 46.47}$$
$$= 11.17 \text{ mH} \approx 12 \text{ mH}$$

(b) ***Capacitor design:***

The output capacitor of the boost converter is determined by,

$$C_1 = \frac{I_{out(max)} * D}{f_s * \Delta V_{out}} \tag{21}$$

where ΔV_{out} is the ripple value of capacitor voltage and f_s is the switching frequency boost converter. The value of ΔV_{out} can be calculated as follows,

$$\Delta V_{out} = (2\% \text{ to } 4\%) * V_{out(\max)} = 0.03 * 46.47$$
$$= 1.4 \text{ Volts} \tag{22}$$

Therefore the value of capacitance can be calculated as,

$$C_1 = \frac{I_{out(\max)} * D}{f_s * \Delta V_{out}} = \frac{5.03 * 0.33}{4000 * 1.4} = 298.17 \ \mu\text{F}$$
$$\approx 330 \ \mu\text{F} \quad \text{(Available in market)}$$

2.4.2. Design of lower boost converter

Since the lower DC/DC boost converter is connected six PV modules in series, the input voltage ($V_{in(low)}$) of the lower boost converter is approximately 214.8 Volts at 1 kW/m^2 and 186.72 Volts at 200 W/m^2(assuming that the minimum irradiance at the installed location). From (7) the output ($V_{out(low)}$) of the lower boost converter should be equal to 278.8 Volts.

So the maximum and minimum duty cycle is given by,

$$\left.\begin{aligned} D_{\max} &= 1 - \frac{V_{in(low)}}{V_{out(low)}} = 1 - \frac{186.72}{278.8} = 0.33 \quad (23a) \\ D_{\min} &= 1 - \frac{V_{in(low)}}{V_{out(low)}} = 1 - \frac{214.8}{278.8} = 0.23 \quad (23b) \end{aligned}\right\} \tag{23}$$

Limit of duty cycles is 0.23–0.33. The duty cycle is not fixed due to the tracking process of the maximum power point voltage. In the above expression the worst condition is the minimum input voltage condition, thus Eq. (23a) is taken into consideration for further designing.

(a) ***Inductor design:***

The value of the inductor used in the upper boost converter is determined as,

$$L_{b2} = \frac{V_{in(low)} * (V_{out(low)} - V_{in(low)})}{(\Delta I_L) * f_s * V_{out(low)}} \quad (24)$$

where ΔI_L is the ripple value of inductor current and f_s is the switching frequency boost converter. The value of ΔI_L can be calculated as follows,

$$\Delta I_L = (2\% \text{ to } 4\%) * I_{out(\max)} * \frac{V_{out(low)}}{V_{in(low)}} \quad (25)$$

$$\Delta I_L = (0.03) * 5.03 * \frac{278.8}{186.72} = 0.23A$$

where $I_{out(\max)}$ is the maximum current delivered from the PV module under maximum irradiance conditions (i.e. at 1 kW/m^2).

Therefore the value of inductance can be calculated as,

$$L_{b2} = \frac{V_{in(low)} * (V_{out(low)} - V_{in(low)})}{(\Delta I_L) * f_s * V_{out(low)}} = \frac{186.72 * (278.8 - 186.72)}{0.23 * 4000 * 278.8} = 67.03 \text{ mH} \approx 70 \text{ mH}$$

(b) ***Capacitor design:***

The output capacitor of the boost converter is determined by,

$$C_{low} = \frac{I_{out(\max)} * D}{f_s * \Delta V_{out(low)}} \quad (26)$$

where ΔV_{out} is the ripple value of capacitor voltage and f_s is the switching frequency boost converter. The value of ΔV_{out} can be calculated as follows,

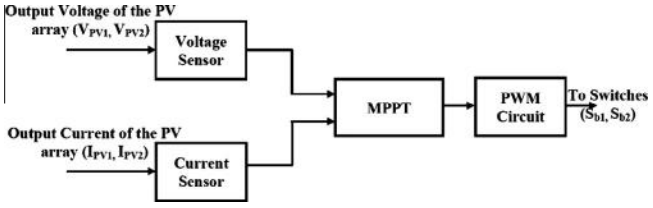

Fig. 5. Control scheme of the DC–DC boost converter.

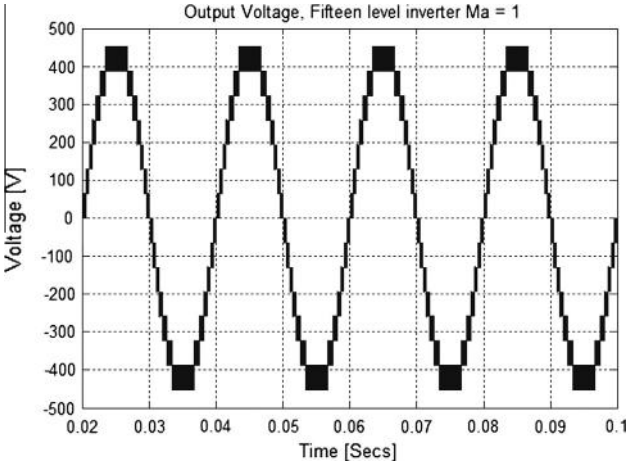

Fig. 6. Inverter output voltage.

$$\Delta V_{out(low)} = (2\% \text{ to } 4\%) * V_{out(max\_up)} = 0.02 * 278.8 = 5.576 \text{ Volts} \quad (27)$$

Therefore the value of capacitance can be calculated as,

$$C_{low} = \frac{I_{out(\max)} * D}{f_s * \Delta V_{out(low)}} = \frac{5.03 * 0.23}{4000 * 5.576} = 51.87 \ \mu\text{F} \approx 68 \ \mu\text{F}$$

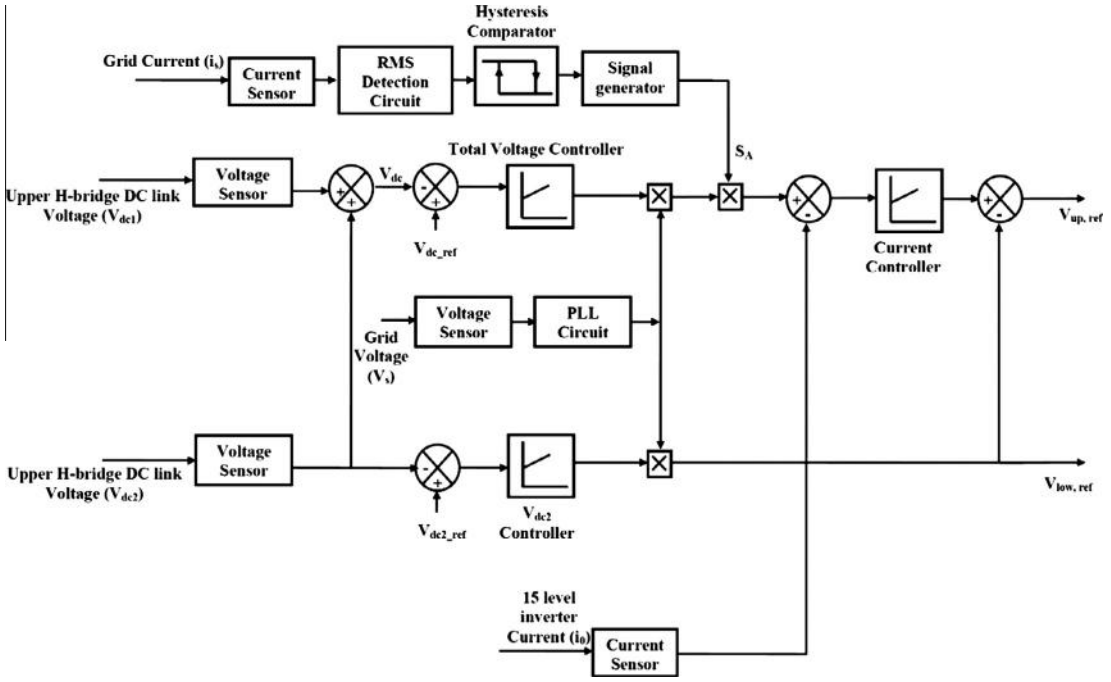

Fig. 4. Control scheme of the fifteen-level inverter.

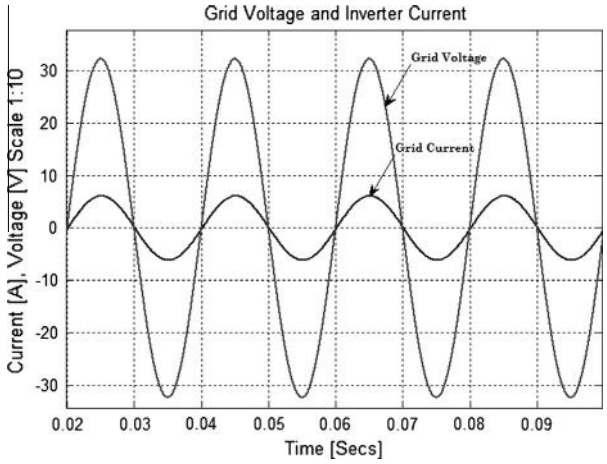

Fig. 7. Grid-voltage and inverter current.

The above value of capacitance is shared by three capacitors in series of equal values. Hence the value of each DC Link capacitance in the lower boost converter is given by,

$$C_2 = C_3 = C_4 = 3 * 68\ \mu\text{F} = 204\ \mu\text{F} \tag{28}$$

2.4.3. Design of AC side filtering Inductance

The filter inductance (L_f) present on the AC side of the inverter is designed based on the following assumptions:

1. The DC bus voltage and AC grid voltage is ripple free.
2. The Modulating signal of the PWM is purely sinusoidal.

The inductor is designed so as to limit the magnitude of the switching current harmonics to a certain percentage of the rated fundamental component. For a good dynamic response, the size of the inductor must be as small as possible. Nevertheless, if the inductor is too small, it cannot suppress the switching ripple current. For high switching frequency and unity power factor operation, the output voltage of the inverter is approximately equal to the grid voltage. The flow of active power is due to a phase angle between the fundamental component of the inverter voltage and the grid voltage.

By simulation, one obtains the magnitude of the dominant voltage harmonic, around the multiples of switching frequency. It is found from the simulation that the dominant harmonic is at 5950 Hz and its value is 6.92 Volts. Considering 3% allowable dominant switching current component, the inductor value can be calculated as

$$X_{f_{sw}} = 2\pi(f_{sw})L_f = \frac{V_{f_{sw}}}{I_{f_{sw}}} \tag{29}$$

$$\Rightarrow L_f = \frac{V_{f_{sw}}}{I_{f_{sw}}}\left(\frac{1}{2\pi f_{sw}}\right)$$

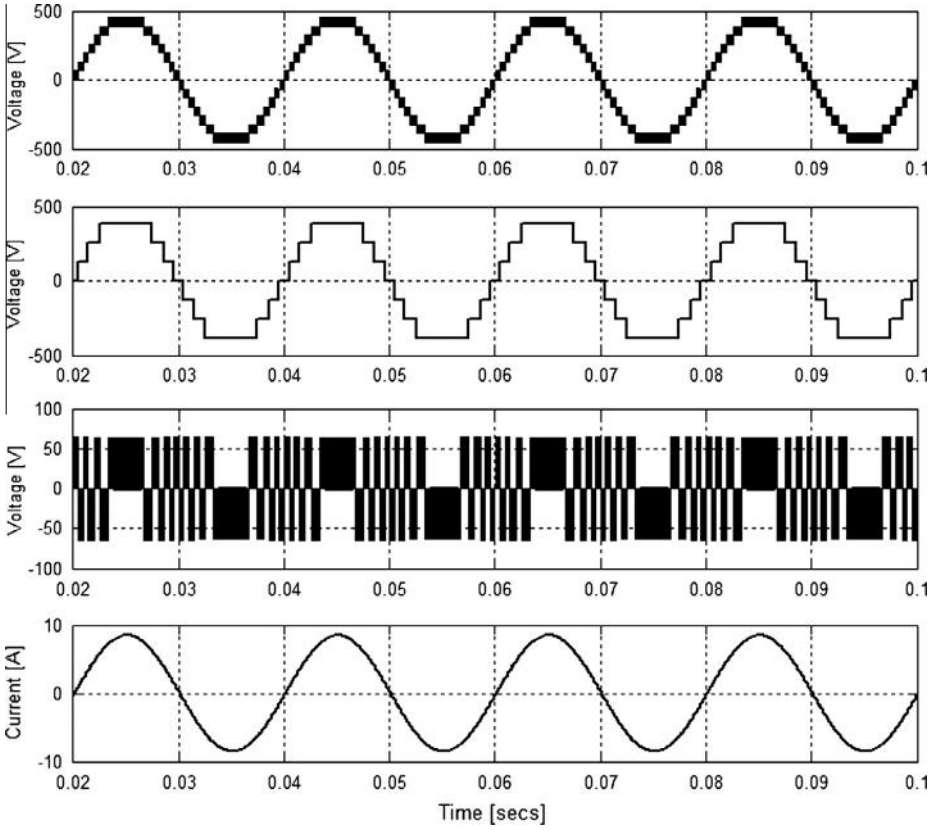

Fig. 8. (a) Inverter-voltage (15 levels Ma = 1), (b) lower inverter voltage, (c) upper inverter voltage (d) inverter current.

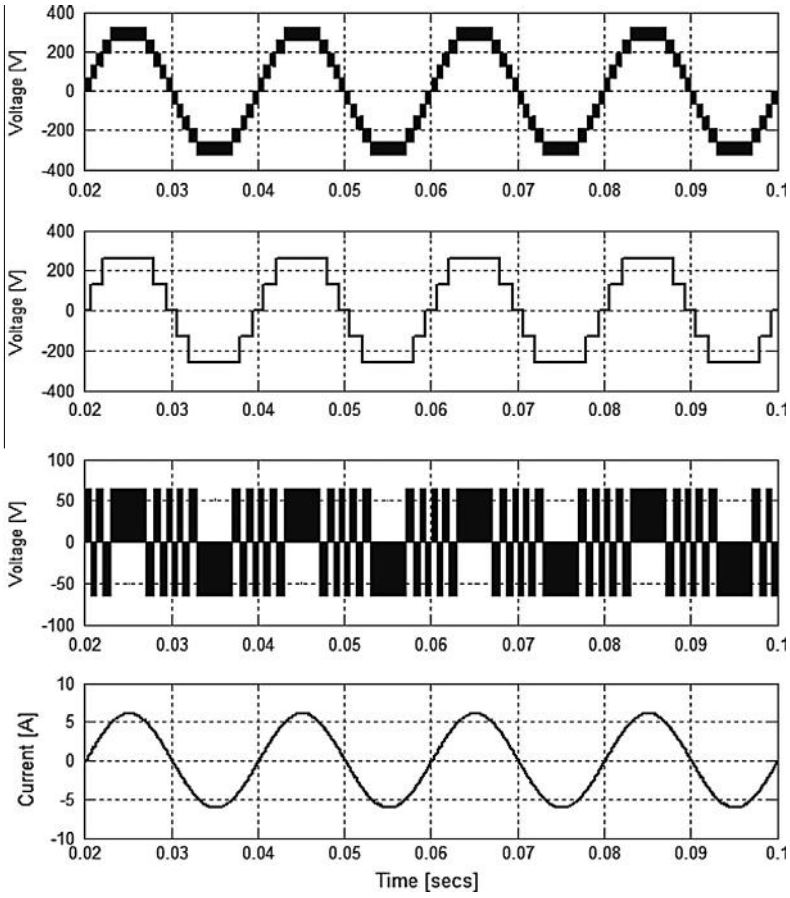

Fig. 9. (a) Inverter-voltage (11 levels Ma = 0.71), (b) lower inverter voltage, (c) upper inverter voltage (d) Inverter current.

From the above figure $V_{f_{sw}} = 6.92\sqrt{2} = 9.786$ and the inverter is designed to deliver maximum of 5.03 A (Maximum Peak Point Current of PV panel used) under rated conditions. Therefore, $I_{f_{sw}} = 5.03\sqrt{2} = 7.11$ Amps Switching frequency of the inverter is $f_{sw} = 5.95$ kHz. Therefore from the above expression

$$L_f = \left[\frac{9.786V}{(0.03 * 5.03A) * \sqrt{2}}\right] * \left(\frac{1}{2\pi * (5950)}\right) = 1.2 \text{ mH}$$

2.5. Control block diagram

The proposed PV based power generation system consists of a dc–dc boost converter and a fifteen-level inverter. The main function of the fifteen-level inverter is to convert the dc power of the PV array into high-quality ac power and pumping it into the grid. The dc–dc boost converter amplifies the output voltage of the PV array and performs the MPPT to extract the maximum output power of the PV array. The controllers of both the fifteen-level inverter and the dc–dc converter are explained as follows.

2.5.1. Fifteen level inverter

Fig. 4 shows the control scheme of fifteen-level inverter. In the operation of the fifteen-level inverter, the dc bus voltages must be regulated to be larger than the peak voltage of the grid and the lower H-bridge dc link voltage must be six times the upper H-bridge dc link voltage. Further, the fifteen-level inverter must inject a sinusoidal current in phase with the utility voltage.

As seen in Fig. 4, the DC link voltages of upper and lower H bridges V_{dc1} and V_{dc2} are detected and then added to obtain a total dc bus voltage V_{dc}. The total dc bus voltage V_{dc} is subtracted from the reference dc bus voltage V_{dc_ref}. The reference dc bus voltage V_{dc_ref} is larger than the peak voltage of the grid. The error voltage (i.e. V_{dc_ref}–V_{dc}) is sent to a total voltage PI controller. Like total voltage PI controller, the lower H-bridge dc link is also controlled by a separate PI controller, V_{dc2} controller. The grid voltage is sensed and then given to a phase-lock loop (PLL) circuit to generate a unity-amplitude sinusoidal signal which is in phase with the grid voltage. The output of the PLL circuit is multiplied with the output of total voltage PI controller and V_{dc2} controller. The output of the V_{dc2} controller is the reference signal of the lower H-bridge inverter.

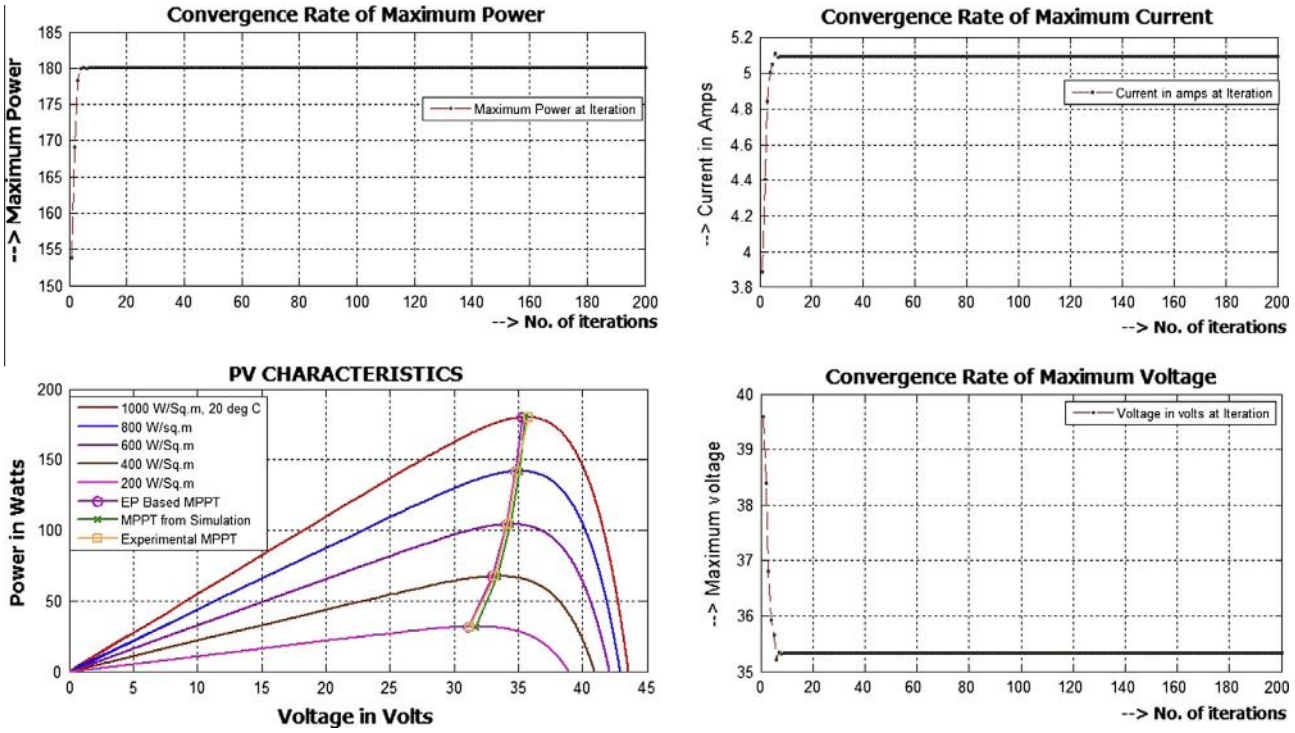

Fig. 10. (a) Objective function tracking of MPP at STC for one PV module. (b) Convergence rate of maximum current at STC (c) PV characteristics for different irradiance with MPP points. (d) Convergence rate of maximum voltage.

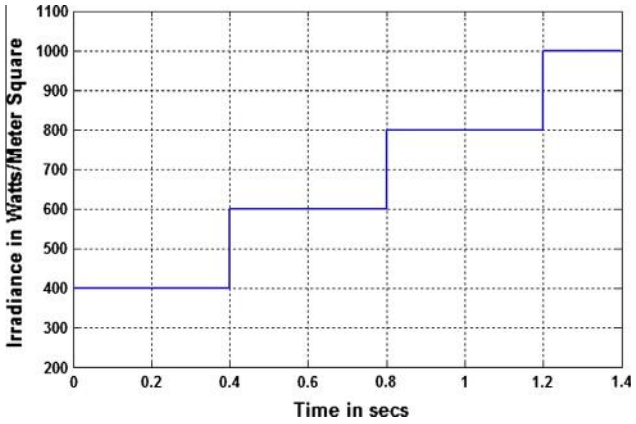

Fig. 11. Step changes in the irradiance.

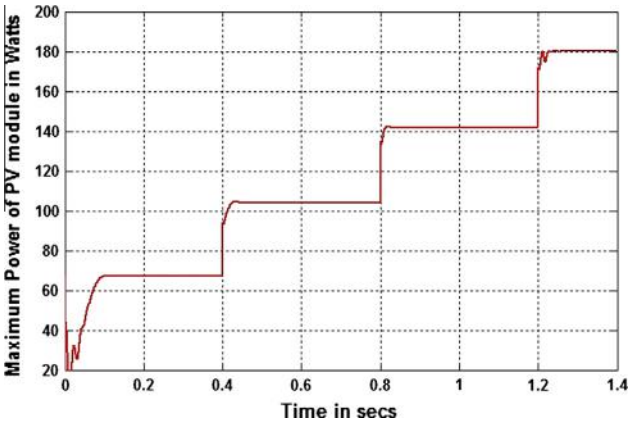

Fig. 12. Output power vs. time of PV panel for step change in irradiance levels.

Further, from Fig. 4, the grid current is sensed and sent to an RMS detection circuit. The information from the RMS detection circuit is given to a hysteresis comparator that has upper and lower threshold limit. Owing to some reasons if the grid fails, then the grid current comes down and reaches a value lower than that of the lower threshold limit of the hysteresis comparator. Under these circumstances, hysteresis comparator output goes high, which opens the switch SW_2 leading to islanding operation. Contradictorily, if the RMS value of the grid current is larger than the higher threshold limit, the output of the hysteresis comparator is low, which means that the grid is normal. The output of the hysteresis comparator is given to a signal generator, whose output is an islanding control signal S_A. The output current of the fifteen-level inverter is sensed by using a current sensor. The reference signal from the multiplier and the sensed inverter current signal are subtracted. The error in current signal is sent to a current-controller. The output of the V_{dc2} controller is subtracted from the current controller current controller output, which results in generation of reference signal to the upper H-bridge inverter.

2.5.2. DC–DC converter

Fig. 5 shows the control scheme of the dc–dc boost converter. The output of the PV array is fed as the input to the

boost converter. Voltage and current of the PV array are sensed and given to the MPPT algorithm. The MPPT algorithm gives the operating voltage of the boost converter. Accordingly, the boost converter switches are switched by the PWM circuit.

3. Simulation and experimental results

3.1. Simulation results

The simulation of the proposed fifteen-level grid-connected PV power generation system is simulated using MATLAB/SIMULINK before it is implemented experimentally as a prototype. The PWM switching patterns for the proposed inverter is developed by using the expressions (4), (7)–(12). The upper inverter is switched at high frequency (i.e. 10 kHz) and the lower inverter is switched at a frequency close to fundamental (i.e. 50 Hz). The upper inverter dc bus voltage is set to 65 Volts and the lower inverter dc bus voltage is set to six times the upper inverter voltage (i.e. 390 Volts). So the net dc link voltage is set to 455 Volts ($>\sqrt{2}\cdot V_{grid}$; in this case V_{grid} is 230 V). The total dc bus voltage should be always greater than $\sqrt{2}$ to inject current into the grid, else current will be injected from the grid into the inverter. Therefore, it is recommended to operate the inverter between modulation indices of 0.71 and 1. Fig. 6 shows the simulated waveform of the proposed 15-level inverter with modulation index of 0.82.

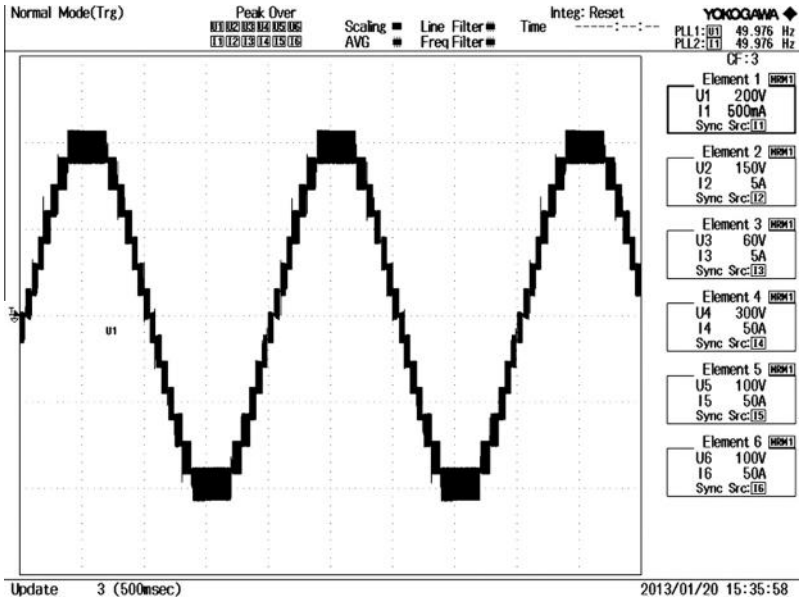

Fig. 13. Inverter output voltage (experimental).

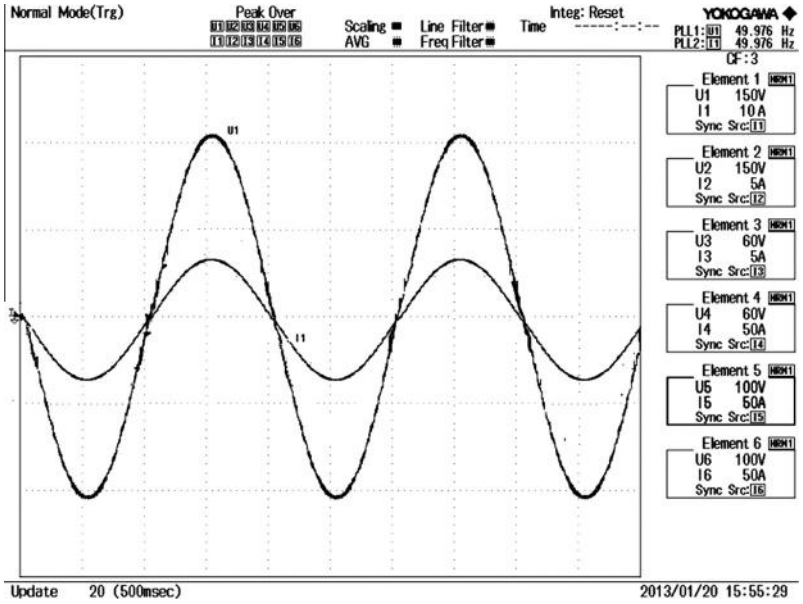

Fig. 14. Grid-voltage and invert current (experimental).

The current injected into the grid is filtered. The filtered current looks very close to a sine wave and is in phase with the grid voltage as shown in Fig. 7.

Figs. 8 and 9 show the simulated waveforms of the proposed grid-connected inverter with modulation indices of 1 and 0.71. Figs. 8 and 9 also include the upper and lower inverter waveform along with the load current. It is evident from these figures that when the modulation index decreases from 1 to 0.71, the number of levels at the inverter terminals also decreases from 15 to 11. The number of solar panels used for the simulation and experiment is seven. The maximum power rating of each PV panel is 180 W at STC as given in Table 2. Therefore, the total power rating of the inverter is 1.26 kW. Fig. 10(a) presents the convergence of the objective function given in Eq. (14). Fig. 10(b and d) show the convergence of current and voltage at the MPP for STC. Fig. 10(c) presents the tracking of MPP by EP algorithm, MATLAB/SIMULINK simulation and the experimental MPP. Table 3 shows summary of the MPP results. From Table 3, it is very clear that the experimental MPP values match the EP based MPP and the simulated MPP values very closely.

In order to validate the performance of the proposed EP based MPPT algorithm, step changes in the irradiance is

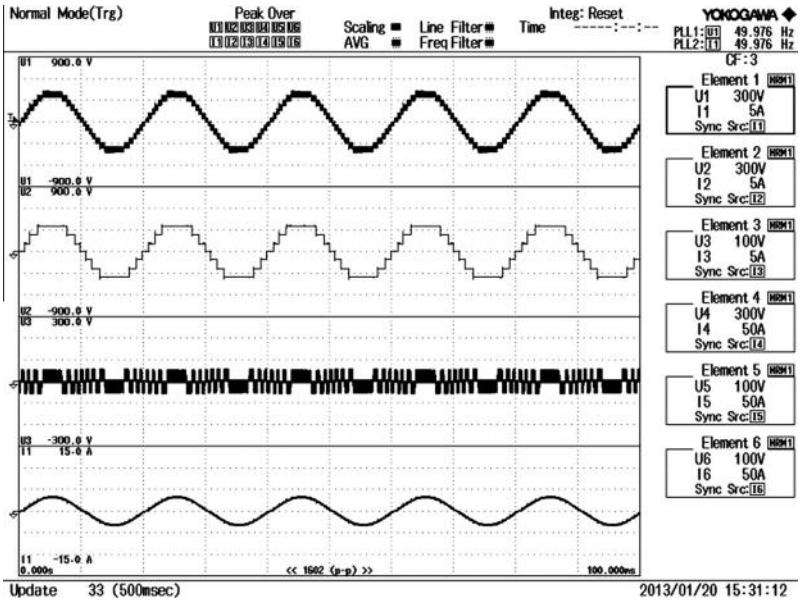

Fig. 15. Experimental waveforms for 15 level Inverter along with upper and lower inverter voltages and load current.

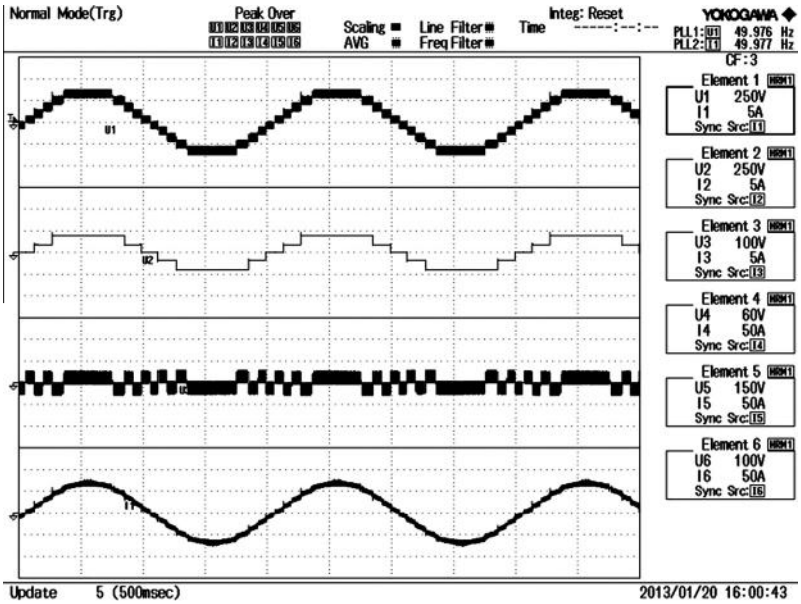

Fig. 16. Experimental waveforms for 11 level Inverter along with upper and lower inverter voltages and load current.

given as shown in Fig. 11. Initially the irradiance is set to 400 W/m^2 and suddenly it is changed to 600 W/m^2 at 0.4 s, 800 W/m^2 at 0.8 s and 1000 W/m^2 at 1.2 s. Fig. 12 shows the corresponding power delivered from the PV panel. From Fig. 12 the maximum power delivered by the PV panel when irradiance is 400 W/m^2 is 67 W, which matches exactly with the numerical values given in Table 3. Similarly the other maximum power point values obtained from Fig. 12 also match with the numerical values of Table 3.

3.2. Experimental results

Hardware prototype is built in the laboratory with the same specifications as in the simulation environment. The upper and lower inverters consist of MKI 80-06T6K series IGBTs. The auxiliary switch used in the lower inverter is FIO50-12BD, a bidirectional device. The photovoltaic panels used are TP180 (TATA BP SOLAR MAKE). Seven number of PV panels are used in the experimental setup. The gate driving signal is developed by using Field Pro-

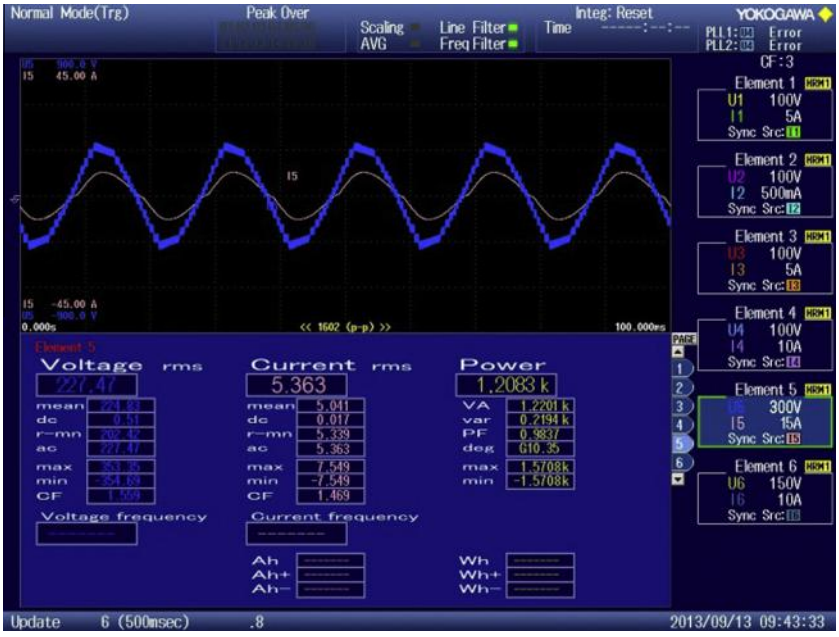

Fig. 17. Voltage and current pumped into the grid when irradiation is 1000 W/m^2.

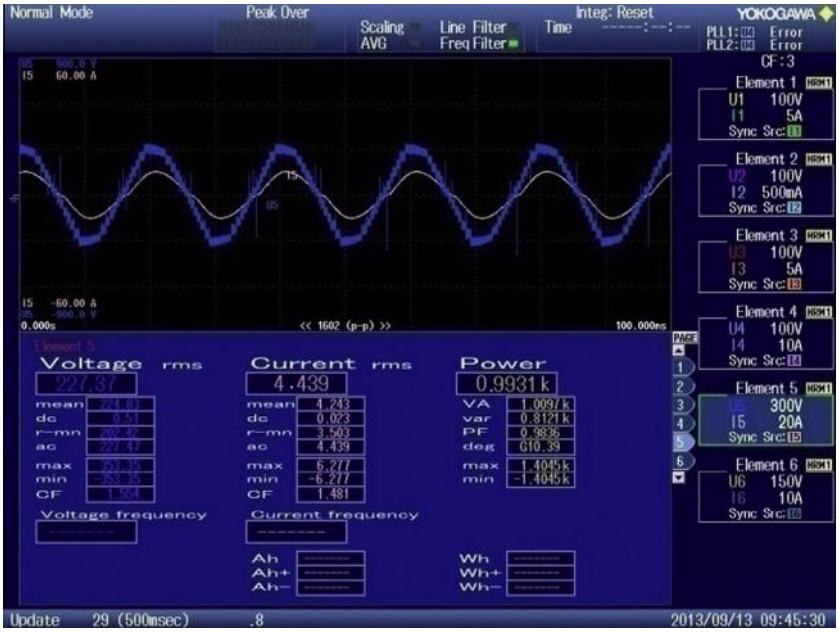

Fig. 18. Voltage and current pumped into the grid when irradiation is 800 W/m^2.

grammable Gate Array (FPGA)-Xilinx SPATRAN 3A DSP. The softwares used to develop programs for SPATRAN 3A DSP are Xilinx ISE Design Siute and Multisim. The voltage and current sensors used are LV25-P and LTF25-NP. Fig. 13 shows the experimental results of the fifteen-level inverter. Fig. 14 shows the experimental waveforms of grid voltage and grid current.

Fig. 15 shows the experimental waveforms of the 15 level inverter for modulation index of 1 along with lower and upper inverter voltages. Load current waveform is also seen. Fig. 16 presents the experimental waveforms of the 11 level inverter for modulation index of 0.71 along with lower and upper inverter voltages and load current waveform. Results of the simulated waveforms (Figs. 6–9) match with that of the experimental results (Figs. 13–16).

Fig. 17 shows the inverter voltage and current fed into the grid when the PV panels are getting irradiation of 1000 W/m^2. The amount of power fed into the grid is 1.20 kW. It is evident from Table 3 that when the irradiation is 1000 W/m^2, each panel delivers 180 W of power. In the developed prototype, there are seven PV panels, so the total power developed by the PV module is 1.26 kW (i.e. 180×7). Similarly, Fig. 18 gives the amount of power fed into the grid when the irradiation is 800 W/m^2. During this weather condition, the maxium power developed by each panel is 141 W. Hence, total power developed by the seven panels put together is 993 W. Hence, it is evident from the numerical values of Figs. 17 and 18 and Table 3, MPPT algorithm works better in delivering power to the grid.

4. Conclusions

This paper has presented a novel single phase multilevel inverter with reduced switching devices and isolated DC sources with evolutionary programming based MPPT algorithm. Simulations are carried out in MATLAB/Simulink and implemented in real time using FPGA board. The simulation and experimental results match perfectly with each other. This proposed inverter system offers the advantage of reduced switching devices and isolated DC sources when compared to the conventional cascaded H bridge inverter. In addition, high frequency switching devices are operated at low voltage and low frequency devices are operated at high voltage. The fifteen-level inverter can perform the functions of regulating the dc bus voltages of upper and lower inverter and convert PV power to ac power with sinusoidal current in phase with the grid voltage. The experimental results verify the developed photovoltaic power generation system, and the fifteen-level inverter achieves the expected performance.

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